PRINCIPLES AND AN EXAMPLE OF HIGHLY ACCELERATED LIFE TEST

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Abstract: This paper describes principles of Highly Accelerated Life Test (HALT) and an example performed on a electronic product operating in the harsh industrial environment. It briefly describes testing methodology, pre-HALT analysis, revealed failure modes, used equipment, and related problems.

Keywords: HALT, reliability, operational limits, design margins, failure modes

1 INTRODUCTION

Fast development, short product life cycles, warranty costs reduction, and product miniaturization are not the only demands of nowadays electronic market. Reliability testing methods should comply to these demands, since accurate reliability forecast can provide information needed for the evaluation of financial risks and market benefits. Old reliability predictions are inaccurate and ineffective; traditional reliability demonstration testing is time consuming, expensive and insufficient within current fast development. In order to avoid these issues, new methods are trying to be integrated to help engineers design a new reliable products within shorter time. Highly Accelerated Life Test (HALT) represents such a method. It reveals weak points and possible failure modes in short testing time (2-5 days) and provides information about product operation in a harsh environment.

2 HIGHLY ACCELERATED LIFE TEST (HALT)

”Quick Learning Cycles must be the religion of thought during product development“, Larry Edson

HALT is a learning tool for effective reliability integration process and it’s widely accepted in the military and commercial applications. It is a qualitative method which improves reliability by subjecting product to stress increasing in steps until a weak point fails. The test is successful when relevant failure modes are found, eliminated and design is improved [2]. Prior to the design changes, each failure mode should be examined by the root cause analysis (RCA) to prove that found failure modes, quickly enhanced during HALT, might appear in the field at lower stress conditions over longer time or due to over-stress.

The principle of HALT is shown in Figure 1 adapted from [5]. While traditional life tests use time as accelerator and strength is decreasing over time, in HALT the accelerator is stress. There can be many types of stress integrated into HALT test plan such as temperature, vibration, voltage, humidity, drop, ESD, pressure, dust, and many others. HALT takes only 2 to 5 days, it is being evaluated at the system or assembly level, and only a few samples (1-6) are usually needed.

By repeating steps of stressing, failure detection, failure analysis and design improvement, HALT pushes the bottom of the bathtub curve down to the fundamental limit of the technology [3].

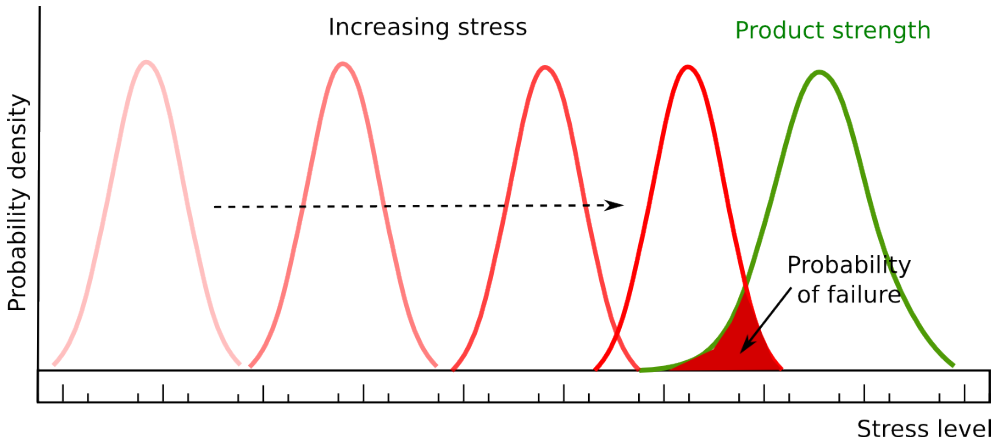

Figure 1: The principle of accelerated stress test such as HALT. Stress is increasing until the fundamental limit of technology (operating or destruct limit) is reached.

2.1 Applications of HALT

HALT is being used to determine potential failure modes and weaknesses by stimulating the failures [1], to duplicate the field failures, to determine the operational (reversible) and destruction (non-reversible) limits, the increase of the product margins = lower failure rate = the increase of reliability, to determine the appropriate stress levels for the ALT, RDT or HASS, a well-grounded comparison of two products, help with the component selection and to verify the material selection and fabricating process, to determine the beginning of wear-out in some cases, to expose hard-to-find defects, or to determine software faults.

Most common uncovered failures are due to [3]: broken leads, socket failures, failed component, screws backed out, incorrect or missing components, incorrect component location, circuit design issue, broken component, tolerance issue, program errors, broken connectors, intermittent connections and many others.

3 PROCEDURE

The typical HALT consists of five steps such as Cold Temperature Step Stress Test, Hot Temperature Step Stress Test, Rapid Thermal Transitions Stress Test (thermal ramp rates of 70 to 100 °C/min), Vibration Step Stress Test (usually 6DoF RS vibration table, up to 75 grms) and Combined Environmental Stress Test (vibration with thermal cycles). More details can be found in [1, 4]. All other necessary tests such as voltage margining, power cycling, or frequency margining should be also involved whenever possible [2].

3.1 Equipment

There are large demands on a chamber suitable for HALT. In Czech Republic, the HALT/HASS chamber that meets these requirements is provided in Brno by Honeywell company. This chamber should provide:

- Fast temperature ramp rates of $\pm$60 to 100 °C/min in a range from -100 to +200 °C. Faster the temperature change, less thermal cycles are needed to achieve the same fatigue. Cooling with liquid nitrogen is usually utilized to meet these requirements.

- Combined environment of vibration and thermal cycles. McLean [1] presented that this kind of stress environment reveals about 20 % of detected failures.
- Repetitive-shocks (RS) vibration table that offers random vibration in six degrees of freedom. This kind of spectrum is especially suitable for electronic equipment since all frequency modes are stimulated at one time. It simultaneously excites bigger components with lower resonant frequency as well as small components with high resonant frequency.
- Online functional monitoring of tested devices allowing observation of interactions between hardware and software in various stress condition.

3.2 Problems

When HALT reveals a wear-out mechanism, it needs to be proven that the warranty period is not affected [3]. Accelerated Life Test (ALT) is a more suitable technique for this purpose.

Repetitive-shock (RS) pneumatic shakers, commonly used in HALT chambers, do not guarantee even excitation and there can be vibration variability across the table. Therefore vibration response should by monitored directly on the product by an accelerometer.

The HALT test sample may not contain hard-to-find defects or rare process problems that are present only in very few products. This problem can be transferred to HASS, where all production is screened.

4 PRACTICAL EXAMPLE

4.1 Objectives and Tested Device

Major objective of the HALT test for a chosen product is to verify the soundness of the product, whether the product can meet customer and company requirements, and to determine the operating and destruct limits.

The tested product is a control electronic circuit board. I/O interface consists of system sensors, switches and interlock circuits. The communication interface is based on RS-485 and provides actual status information and details of control. Temperature operating range is -40 °C to +60 °C and environmental rating for continuous vibration is 0.5 g.

4.2 Pre-HALT Analysis

FMECA (Failure mode, effects and criticality analysis) was discussed to reveal potential failure modes and types of stresses that should be integrated into the testing procedure. Since main causes of these failures are temperature and vibration, no other stress types were incorporated into the test procedure. Test was carried out on two samples. The standard testing procedure as described in Section 3 was performed.

Functional Test Requirements: during HALT, the product is powered on and continuously monitored with external equipment. National Instruments multi-functional DAQ system was used for this purposes. Complete functional test is performed at each stress step after reaching thermal equilibrium. The product is controlled by digital inputs and passed through all program states (WAIT, RUN, etc.). The state of inputs/outputs, actual power consumption and communication messages were monitored and logged continuously. If any anomaly was discovered, the procedure was paused, stress level decreased and root cause analysis performed. The device operation (state of LEDs) during the stress exposures was also monitored visually. All variables such as temperature, vibration, power consumption and system status information were logged into a file.

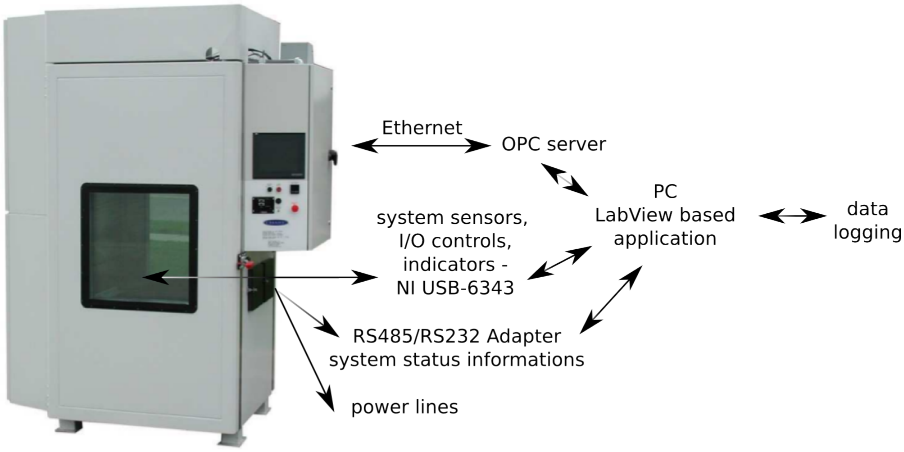

Figure 2: HALT chamber Chart Real-30 and connection diagram for functional test

In order to understand how the product is stressed, vibration response was measured by a three-axis accelerometer. The accelerometer is placed in the center of the board during vibration stress test. Thermocouples are placed on the master microcontroller and transformer.

4.3 Results And Found Failures

Cold stress: The device ”freezes“ below -80 °C. After reseting the device, correct input conditions are detected during initialization, but there is no response to input changes after that. Communication is lost. This failure occurred due to a microcontroller, whose specified temperature range is from -40 °C to +85 °C. The cold step stress test did not cause any destructive failure. The lower operating temperature limit is -80 °C.

Hot step stress: At the temperature of 150 °C all LEDs start to blink, there is no reaction to input changes and the device does not communicate with the PC through the diagnostic interface. Plastic packages starts to melt above 155 °C. There is no reason to continue increasing temperature since the fundamental limit of technology is reached. Temperature related failures are caused by over-stress. Therefore, they are not expected during normal life. The upper operating temperature limit is +145 °C.

Rapid Temperature Cycling: There were no problems noted during temperature cycling between -80 and 145 °C.

Vibration stress: Two protection varistors and a capacitor fell off the board as can be seen in Figure 3. The exact time of failure is not known as the device is able to work without them. A hard failure, a fracture between the connection lead of the transformer and the wound of the primary coil, occurred at 65 grms. This is well known failure mode. Since vibration fatigue is the cumulative failure mechanism, further analysis is needed to determine expected time to failure in intended use environment. The operating and destruct vibration limit is 65 grms.

Combined Environment: There were several fractures between connection leads and the wound wire of the core coil. Another capacitor fell off. At the end of the test, broken connections were fixed and the device worked properly.

5 DISCUSSION

The accuracy of operating limits depends on the number of samples, size of stress increments and the precision of stress level. For example 80% confidence bound estimate of upper operating limit

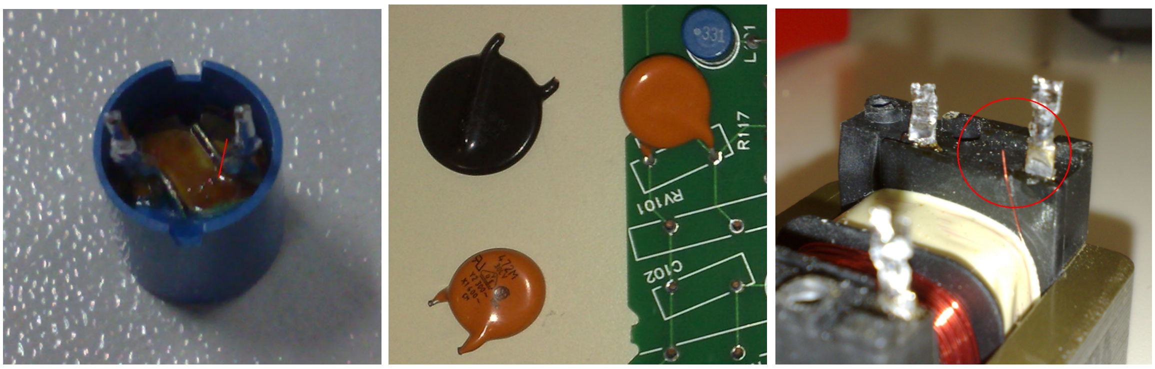

Figure 3: Hard failures

from two samples with upper temperature operating limit of 140 and 145 °C is +141 °C. Temperature control of the chamber Chart Real 30 offers ±1 °C and ±1 gRMS within 1 min of settling for vibration. However it depends on control overshoot during temperature stabilization and the coarseness of the steps. The accuracy of results is estimated based on previous tests to ±5 °C. Further design improvement can focus on the coil and transformer selection and comparison of different manufacturers. HALT is a perfect tool for doing this. Broken connectors of capacitors and varistors can by prevented by applying glue between the PCB board and component, or by fixing components together. This type of failure is not expected during service life.

6 CONCLUSION

Despite HALT does not replace life tests, it improves reliability by finding and correcting weaknesses, broadens margin between product strength and field stresses, determines operational margins, and indirectly shortens developing time. HALT is a great learning tool that offers valuable feedback about product behavior under different loads and working conditions. It enables to find failure sooner than after weeks of verification testing, and thus saves costs and time.

The product with the temperature operating limit of -80°C to +145 °C and vibration limit of 65 grms can be considered as robust from the HALT test perspective. Found failures were caused by individual components because the fundamental limit of technology was reached. All discovered issues occurred at significantly higher conditions than specified operational range and the product has sufficient operational margins.

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