FPGA BASED DELTA-SIGMA ANALOG TO DIGITAL CONVERTER

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Abstract: The article presents an unconventional approach to perform delta sigma A/D conversion. Splitting the first order delta sigma converter into analog and digital part makes an illustrative laboratory classes aid for undergraduate students as well as inviting discussion about the applicability in real world applications. The analog part is realized using basic analog integrated circuits, while the digital part is implemented using FPGA. This allows FPGA to influence the converter's properties and makes further processing easier.

Keywords: Delta Sigma, Analog to Digital Converter, FPGA, Xilinx, MicroBlaze

1 INTRODUCTION

The Delta-Sigma analog to digital converters have found its way into a wide range of modern applications including process control, instrumentation and audio equipment. The high-resolution, good linearity, noise suppresion and bandwidth up to units of MHz make them a strong competitor to dual-slope integrating ADCs as well as successive approximation ADCs.

The converter consists of simple analog electronics, but rather complex digital computational circuitry. This lead the author to the idea presented in this article – having the analog circuitry built using basic analog integrated circuits, while performing the digital computations in an FPGA (Field Programmable Gate Array). The resulting design is proposed as a laboratory classes aid for undergraduate students, therefore a simple comprehensible design is favoured to overall performance.

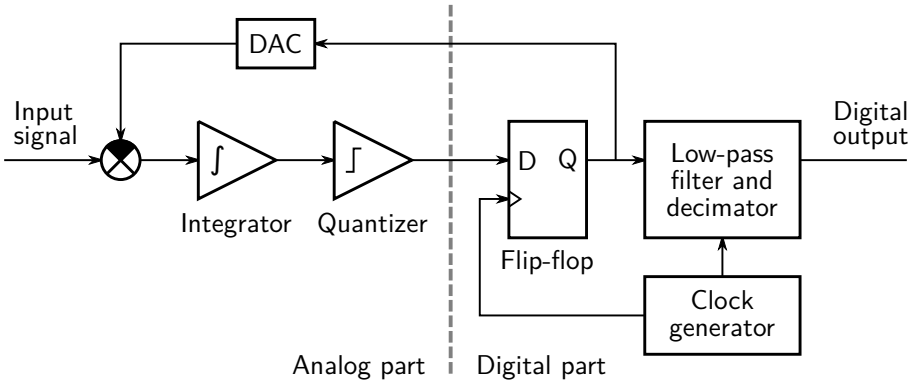

Figure 1: Block Diagram of Delta-Sigma ADC

Figure 1 illustrates the well-known principle of analog/digital conversion based on a delta-sigma modulation. The analog part consists of a single integrator, a 1-bit ADC (quantizer) and a 1-bit DAC. The digital part closes the negative feedback loop, shaping the noise, limiting the bandwidth and decimating the digitized signal.

1.1 OVERSAMPLING

By definition, an analog to digital conversion introduces a quantization noise – random errors of magnitude up to ±LSB. Figure 2 illustrates the FFT analysis of the digitized signal. The noise extends from DC to $f_S/2$, where f_S is the sampling frequency.

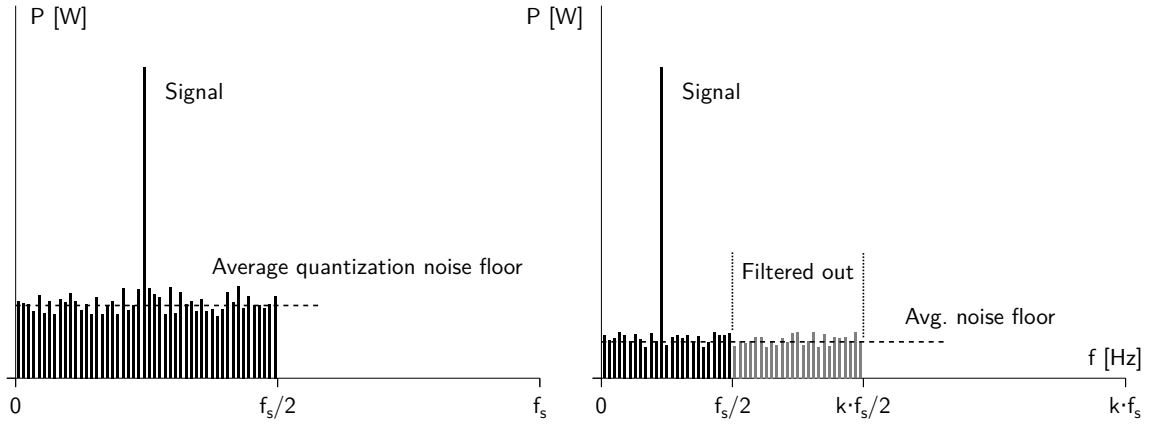

Figure 2: Quantization Noise

The quantization noise limits the signal to noise ratio (SNR) of an N-bit ADC to approximately SNR = 6.02 N + 1.76 dB. By increasing the sampling frequency by the oversampling ratio k, the SNR remains the same, but the noise energy spreads across a wider frequency range. Delta-sigma converters exploit this effect by removing frequencies above f_S using a digital filter.

1.2 NOISE SHAPING

To gain one additional bit (increase the SNR by 6 dB), oversampling by a factor-of-4 is necessary, making the high resolution ADCs out of the question. To overcome this limitation, delta-sigma converters take advantage of noise shaping. Having the feedback loop closed, the integrator acts as a lowpass filter to the input signal and a highpass filter to the quantization noise, causing it to be pushed into higher frequencies [1].

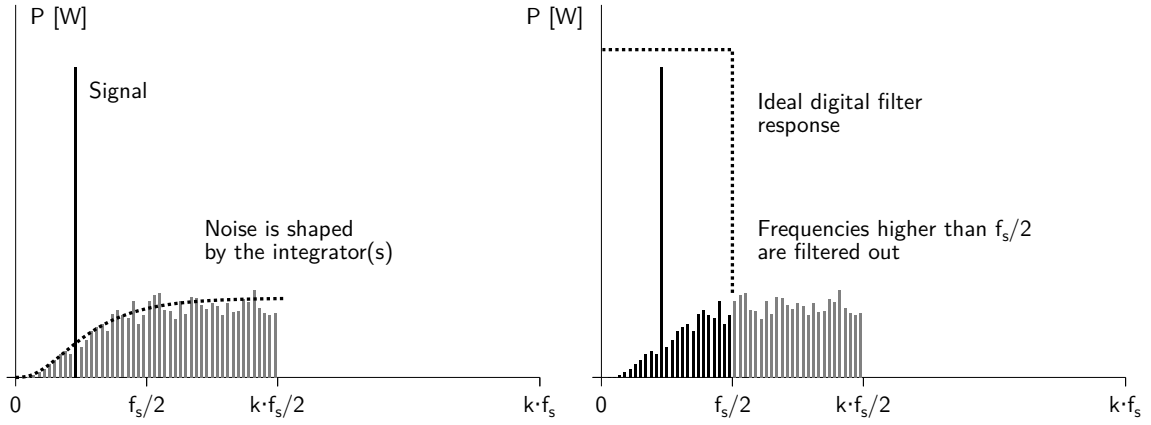

Figure 3: Noise Shaping

Increasing the order of delta sigma modulator results in better noise shaping performance, gaining the same SNR with lower oversampling factor. This allows to achieve higher resolution and bandwidth.

1.3 DIGITAL FILTERING

Prior to downsampling the signal from analog circuitry, a low-pass anti-aliasing digital filter is employed. To maintain a good SNR, it is desirable to suppress as much of the undesired spectrum (above the Nyquist frequency $f_S/2$) as possible to minimize negative effects of spectral folding caused by decimation.

In reality, a compromise between time and frequency domain behaviour has to be considered along with specific application requirements, hardware complexity and costs. In general, a very popular decimation structure is the sinc filter. For 2nd order modulators, the sinc^3 filter is considered close to optimum [2].

2 ANALOG CIRCUITRY

The topology of the analog part follows the block schematic depicted in Figure 1. The operational amplifier OZ2 implements the integrator, the comparator OZ3 acts as the quantizer (1-bit ADC), while OZ4 driven current drain IC1 serves as the 1-bit DAC.

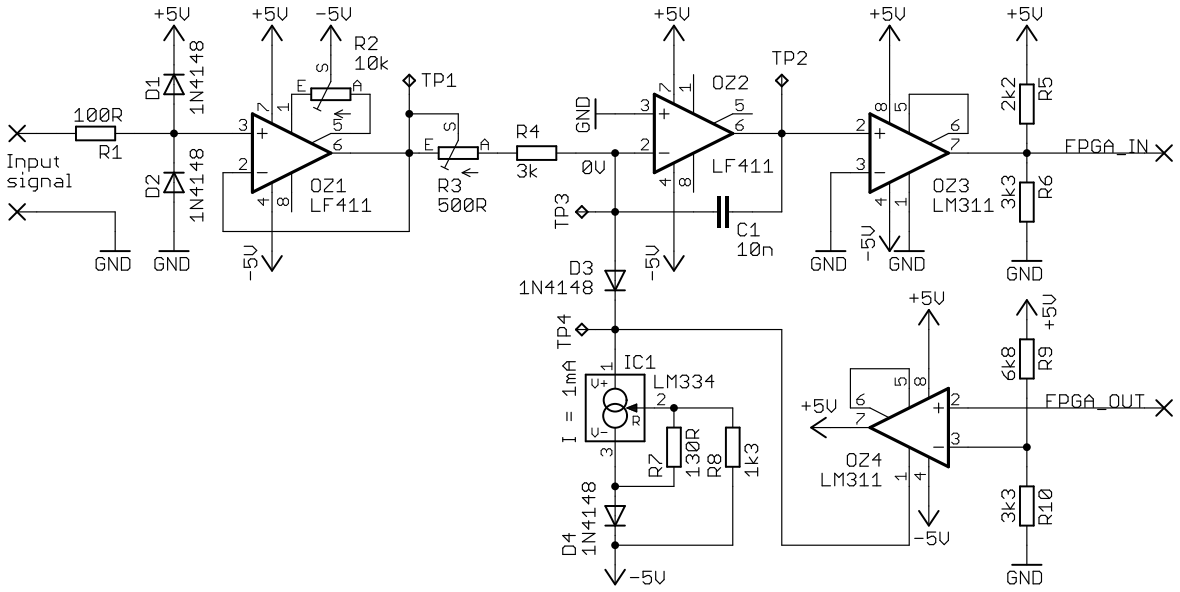

Figure 4: Schematic of Analog Circuitry

The input characteristics of the A/D converter are defined by the signal conditioning stage comprised of the diode clamping circuit and the voltage follower OZ1. The intended input voltage range is 0 V to 3.3 V. The offset voltage can be balanced using R2, enabling to set the zero of the A/D converter as a whole.

The operational amplifier OZ2 acts as an integrator. Thanks to the negative feedback, a virtual zero at TP3 is maintained and current flowing through R3-R4 is linearly proportional to OZ1's output voltage. The variable resistor R3 allows to fine-tune the voltage/current conversion ration, which determines the ADC's input voltage swing.

Considering R3+R4 set to 3300 Ω, the input voltage range 0 V to 3.3 V corresponds to OZ1's output current ranging from 0 mA to 1 mA. Time constant of the integrator is $T = (R3 + R4) \cdot C1 = 330\ \mu$s.

The comparator OZ4 acts as a voltage level shifter. It allows to divert the current flowing through the temperature compensated current drain IC1. This 1-bit DAC is driven by FPGA according to the polarity of OZ2's output voltage.

3 DECIMATION

To perform low-pass digital filtering, the N-point moving-average filter has been used, also called sinc^1. With comparison to the frequently used sinc^3 filter, it is easier to implement and provides better performance in time domain, allowing to measure low frequency signals precisely with faster settling time. On the other hand, it does not excel in frequency domain, making the ADC more sensitive to high frequency noise.

The filter's output in time can be expressed as

$$y(n) = \frac{1}{N} \sum_{k=0}^{N-1} x(n-k) \tag{1}$$

It has been shown, that y(n) can be obtained by adding the current input sample x(n) and subtracting the oldest one x(n-N) from the previous output average y(n-1). The advantage of the recursive implementation is that only one addition and one subtraction are required per output sample, regardless of the delay length D. [3]

$$y(n) = y(n-1) + \frac{1}{N}\left[x(n) - x(n-N)\right] \tag{2}$$

Ignoring the 1/N scaling, we obtain the classic form of the 1st-order CIC filter. Having the Shannon-Nyquist sampling theorem criterion satisfied, it is safe to perform downsampling.

4 EVALUATION

The functionality and performance of the designed delta-sigma ADC have been evaluated using an Avnet Spartan 3A Evaluation Kit and soft microcontroller Xilinx MicroBlaze. The decimation filter logic has been equipped with PLB interface, allowing the soft microcontroller to treat the A/D converter as a memory mapped peripheral.

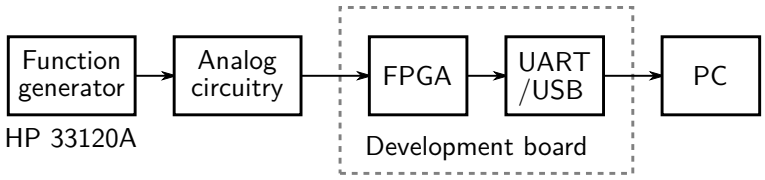

Figure 5: Block Diagram of Measurement Configuration

The end-point integral nonlinearity of ADC and SMRR (Series Mode Rejection Ratio) as a function of noise frequency have been evaluated. The measurement has been performed using sampling frequencies of 10 kHz and 204.92 kHz, 12 bits resolution and 4096 oversampling.

Integral nonlinearity (INL) is a measure of the deviation of an ADC's transfer function from a straight line. It does not consider offset and gain errors.

f_S [kHz]	INL [mV]	INL [LSB]
10.00	4.6	5.7
204.92	140.6	174.5

Table 1: Integral Nonlinearity of ADC

While the integral nonlinearity at $f_S = 10$ kHz is being acceptable for basic measurements, a pronounced distortion can be observed at $f_S = 204.92$ kHz.

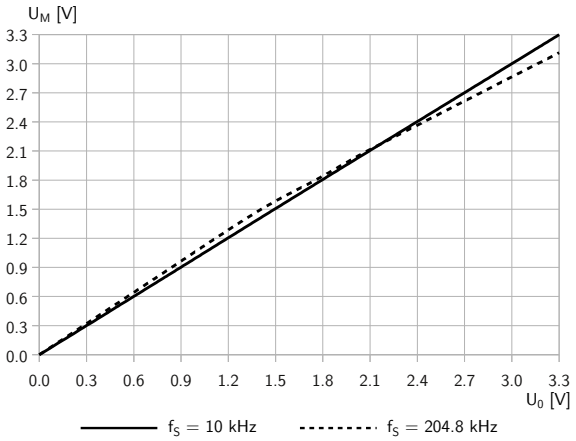

Figure 6: Transfer Function of ADC

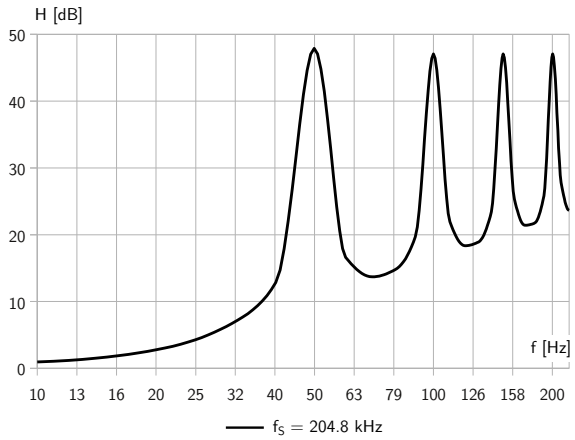

Figure 7: Series Mode Rejection Ratio

Series Mode Rejection Ratio reflects the frequency characteristics of the moving-average filter. For $f_S = 204.92$ kHz, the best noise rejection can be observed at multiplies of 50 Hz. The SMRR for $f = 50$ Hz equals -47.8 dB. On the other hand, only SMRR = -13.7 dB is provided at $f = 70$ Hz.

5 CONCLUSION

With reference to the provided evaluation, it is obvious that the simple implementation cannot compete with state of the art integrated solutions. The disadvantage arises from circuit's form factor introducing higher parasitic effects and overall design simplicity.

Despite the mentioned downsides, the design is appealing for its tight integration into FPGA. It allows to configure converter properties easily, use application specific digital filter, dynamic reconfiguration or integrate into soft microcontroller system easily.

When used as the laboratory classes aid, it allows students to explore the internals of the delta-sigma converter's analog part as well as experiment with the digital design. The hardware makes possible to evaluate the real circuit behaviour along with all its imperfections and makes the classes more appealing.

ACKNOWLEDGEMENT

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