ADVANCED SECURE MEMORY PROGRAMMER FOR INTEGRATED POTENTIOSTAT ANALYZER

Martin Magát
Doctoral Study Programme (1) , FEEC BUT
E-mail: martin.magat@phd.feec.vutbr.cz

Supervised by: Radimír Vrba
E-mail: vrbar@feec.vutbr.cz

ABSTRACT

This paper describes a design of an advanced secure memory programmer for remote control of an integrated potentiostat. The programmer can read data from integrated potentiostat memory and write data into this memory safely and in secure mode. This is required because standard PROM memory integrated in the potentiostat can cause damage when writing is repeated. The core of the secure programmer is designed using the ATMEL ATtiny 2313 microcontroller. The programmer is remotely controlled by a personal computer via a standard USB interface.

1. SECURE PROGRAMMER DESCRIPTION

The programmer consists of two essential parts. The first one is a programmer itself and the other is control software developed for Windows XP. The programmer runs fully under software control only.

1.1. CONTROL SOFTWARE

The control software is designed for easy and simple use and has four sections: *Device*, *Status*, *Data* and *Control Buttons*. The *Device* section contains components for the choice of programming devices and connecting and disconnecting them to the programmer. In *Status* section the status of connection to the programmer is shown. The very important section is *Data*. In this one read data from integrated potentiostat memory is shown and user can mark the bits which will be written. The last section *Control Buttons* contains buttons for reading and writing to integrated potentiostat memory.

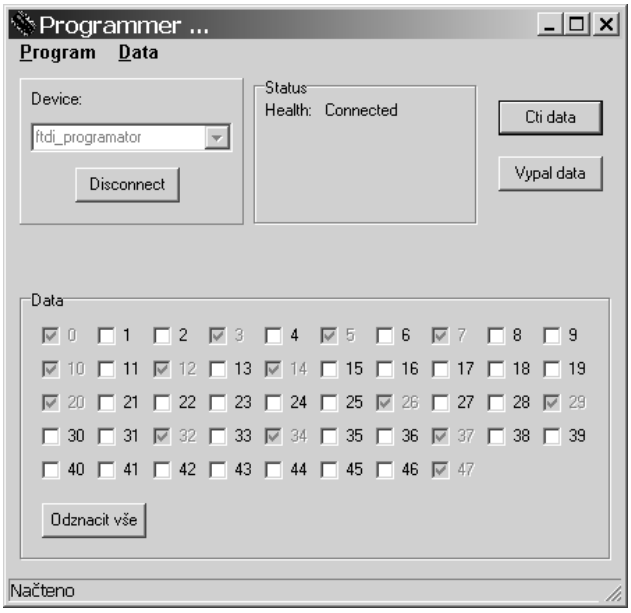

Fig. 1: Screenshot of interactive control software for integrated potentiostat memory programmer

Fig. 1 depicts the situation when some bits have been previously written. Previously written bits are disabled for new writing. Data from integrated potentiostat memory are read automatically after all writings into this memory.

1.2. PROGRAMMER

The core of the integrated potentiostat memory is created by ATMEL ATtiny2313 microcontroller replacing AT90S2313. It is a very simple microcontroller which was chosen because it features required parameters, like 2K Bytes size of system self programmable flash memory, 18 programmable I/O lines and full duplex USART.

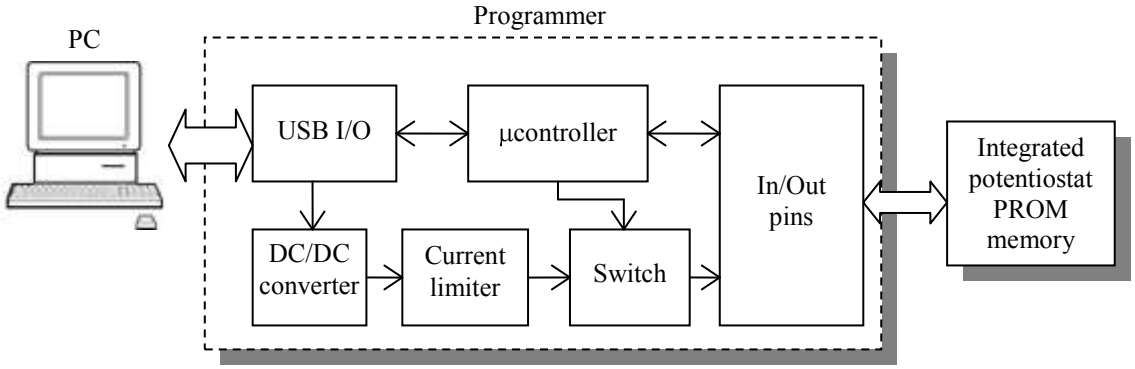

Fig. 2: Programmer block diagram

The memory requires programming voltage in the range 15 to 17 V. That is why there is a DC/DC converter inside the programmer. This converter is a step-up converter which converts voltage from USB (above 5 V) to programming voltage of 16 V. There is a DC/DC converter plugged at the output of the current limiter. The current limiter protects programmed memory against abnormal current.

1.3. DATA WRITING PROCESS

For correct writing into the integrated potentiostat memory it is necessary to observe the following writing sequence exactly.

First the supply voltage for integrated potentiostat is activated (VDD), followed by the first pulse in clock signal (SC) which resets integrated potentiostat. Then programming voltage switching on which takes the integrated potentiostat to writing mode. The first logical bit to the integrated potentiostat shift register is shifted after signal DZAP is driven on and after the pulse in the clock signal. Now the number of pulses in the clock signal indicates the position of the memory bit which will be written. The signal SD copies the content of the integrated potentiostat shift register to the PROM cells and BCTRL switches the programming voltage to this memory cells. And now the writing process is activated by enabling WE signal. Then the programming voltage is disconnected by BCTRL (go to 0). The writing process into the memory cell is finished. The technology requires all the memory cells to be burnt separately. After writing one bit another bit has to be chosen for writing by setting the corresponding number of pulses in the clock signal. After the programming the last bit the power supply is switched off. An example of writing process is show in

Fig. **3**.

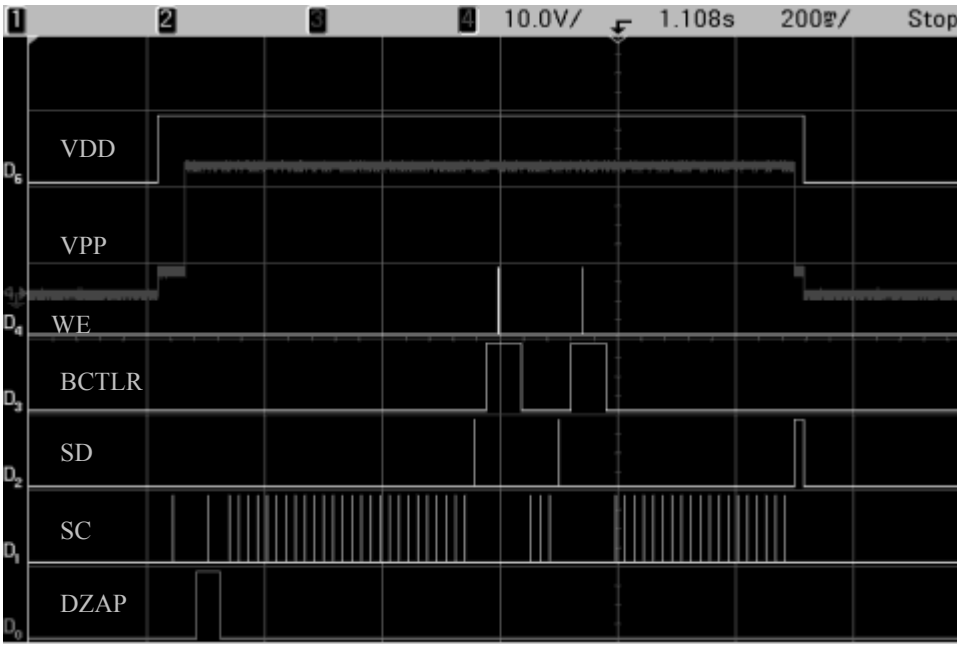

Fig. 3: Writing memory cells 26 and 29

1.4. DATA READING PROCESS

The example of reading sequence is shown in

Fig. 4. There is shown in this figure that memory cells 0, 5, 10, 12, 20, 26, 29 are written. No reconnecting or other manipulation with integrated potentiostat is required. The reading sequence starts by switching power supply voltage (VDD) on. The first three clock pulses (on SC) reset the integrated potentiostat and its shift register. Data is shifted to the data pin

(SD) by another pulse in the clock signal. After reading the last bit the power supply is switched off again.

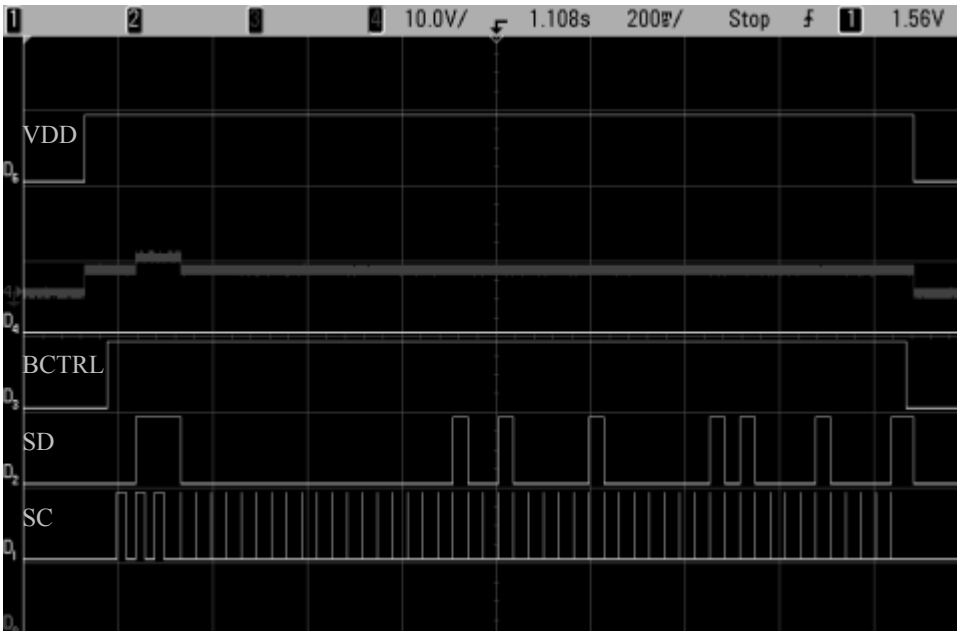

Fig. 4: Example of reading from memory

1.5. COMMUNICATION BETWEEN MICROCONTROLLER AND CONTROL SOFTWARE

USB I/O part of the programmer has been created by FTDI 232BM. This part communicates with the microcontroller via USART. The program in microcontroller is very small because the microcontroller runs instructions which were received from USART (USB). The instructions are very simple and include basic parts of writing and reading processes. USART is working in full duplex mode and basic diagram of communication process is shown in **Fig. 5**.

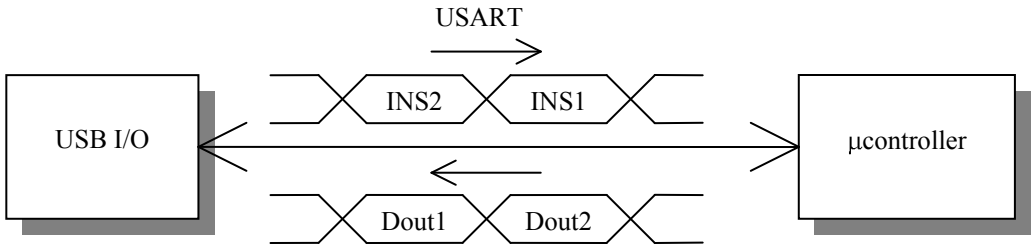

Fig. 5: Data transfer diagram

Timing in the communication protocol is very critical. The latency during data transfer on USB interface should be considered.

2. CONCLUSION

Described advanced secure programmer can program integrated potentiostat memory in remote control mode. The programmer can check which memory cells are programmed. The programmer is controlled by a personal computer via USB interface. No external power source is required.

ACKNOWLEDGEMENT

Funding for this work was provided by the Czech Science Foundation under the contracts GACR 102/06/1624 and GACR 202/05/0607, Czech Ministry of Education in the frame of Research Program MSM0021630503 MIKROSYN New Trends in Microelectronic Systems and Nanotechnologies and partly supported by the grants 1QS201710508 and FRVS 2503/2007.

REFERENCES

[1] Steffan, P., Prokop, R., Vrba, R., Fujcik, H., Haze, J., Krejci, J. ASIC Measurement System for TFT, International Conference on Sensors and New Techniques in Pharmaceutical and Biomedical Research, September, KualaLumpur, 2005, pp. 344 - 347, ISBN 0-7803-9371-6

[2] P.Steffan, J.Haze, R.Vrba: New Integrated Measurement System for Electrochemistry Microsensors, WSEAS Transactions on Circuits, ISSN 1109-2734, 2004, No. 9, pp. 1962 -1964