AN ADVANCED SCR PROTECTIVE STRUCTURE AGAINST ESD STRESS

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ABSTRACT

ESD (electrostatic discharge) protection structures act as a protection of integrated circuits against parasitic electrostatic discharge events. They are located on input or output (I/O) pads. The use of such structures provides better robustness against ESD but also a number of secondary parasitic effects which limit the circuit performance. These effects limit bandwidth of processed signals, cause bigger noise or lower gain. Among often used structures belong structures known as SCR (silicon controlled rectifier). Structures like SCR have some disadvantages, therefore they can not be universally usable. This text is dealing with an advanced SCR structure, which overcomes disadvantages of conventional SCR protection cell. Physical principle of this new structure allows required features tuning by geometrical adjustments only

1. INTRODUCTION

Fig.1. illustrates principal connection of ESD protection.[2] The protection cells are either single path or dual path at its I/O. A random ESD stress goes through this structure to the ground and the core circuit is not endangered.

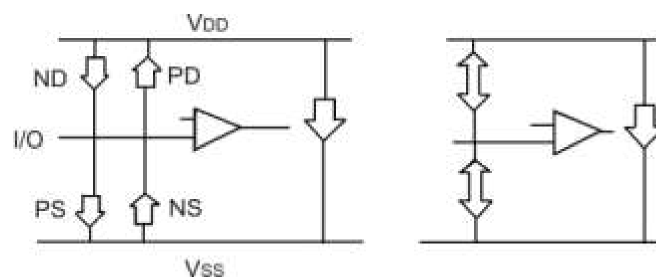

Fig 1: Single path and Dual path ESD protection structures with supply clamp on the right

Fig.1 on the left side shows single path at I/O ESD protection with one-directional supply clamp. In the middle is dual path at I/O ESD protection with one-directional supply clamp. Both types of protection (single or dual path I/O and supply clamp) must not be active during normal circuit performance. The protections must be active only during ESD event.

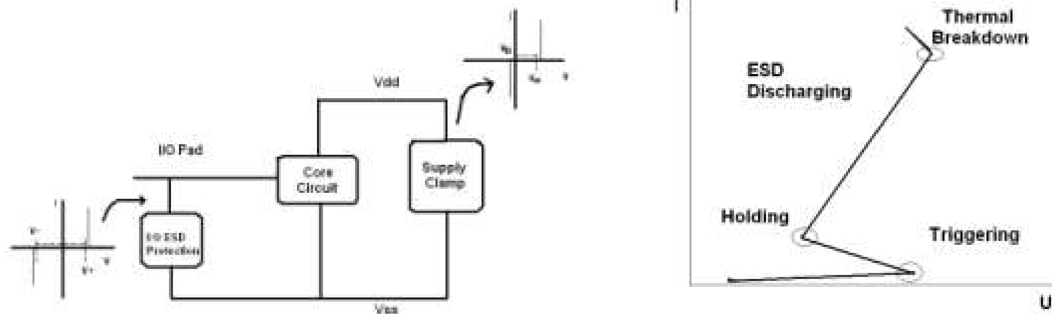

Fig 2: I/O ESD protection and supply clamp on the left, required A/V characteristics of ESD device on the right

Required A/V characteristic (fig.2 right) of ESD protection device should fulfil conditions like: The value of leakage current is low, the ESD current in the area of snapback is big, big robustness of ESD cell. The other needed parameters are: Triggering voltage adjustability, holding voltage adjustability, the ESD cell must not be destroyed during an ESD stress, parasitic effects must be minimal.

2. ANALYSIS

2.1. CONVENTIONAL SILICON CONTROLLED RECTIFIER (SCR)

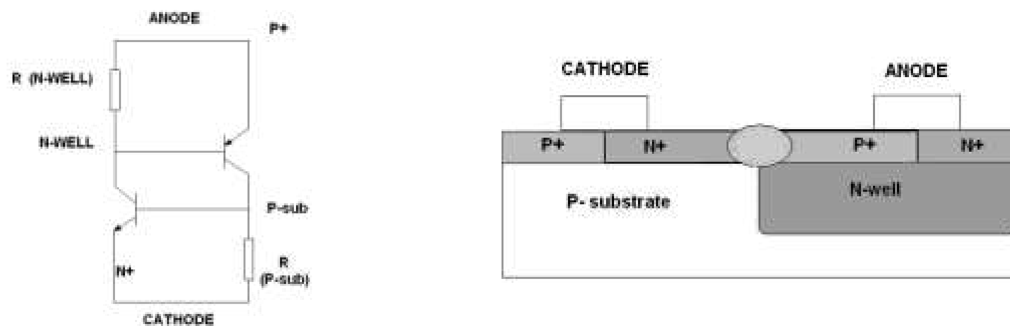

Fig 3: The basic SCR structure.[4],[5]

In fig.3 is seen the basic structure of conventional SCR protection. The resistances in the P-substrate and in the N-well are needed to provide a voltage drop to trigger two bipolar transistors. The areas P+ and N+ under the cathode and anode are used to extend contacts of the resistances. A disadvantage is difficulty to optimize triggering voltage, holding voltage and resistance R_{ON} in this device in such a way to reach the requirements mentioned above.

2.2. BASIC STRUCTURE OF ADVANCED SCR DEVICE

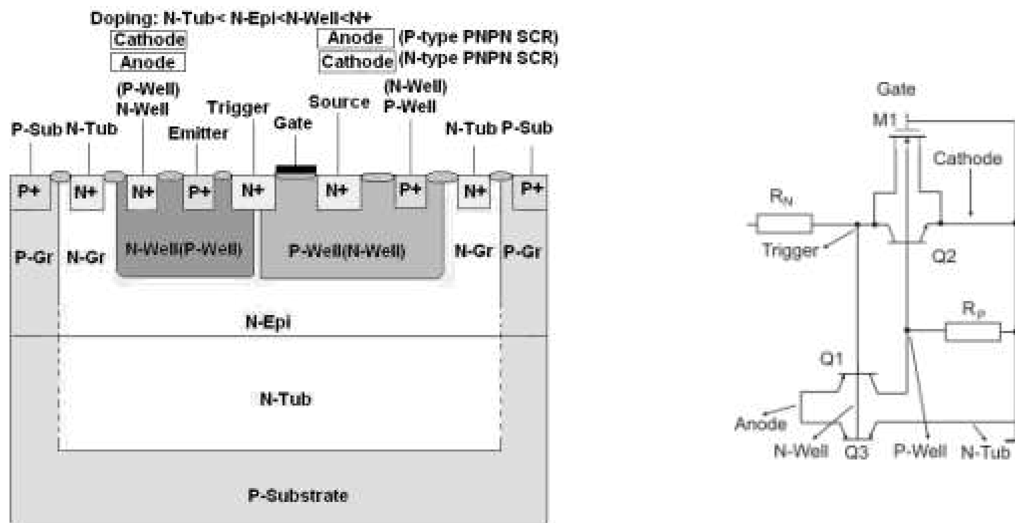

Fig 4: Structure and scheme of an advanced ESD device,[1],[3].

Fig.4 shows the basic structure of an advanced ESD protection, which is based on SCR cell. The triggering terminal is opened. It is possible to connect it to anode to trigger SCR faster if it is necessary. The gate can be replaced by the FET to change triggering voltage a to prevent oxide breakdown. This gate terminal is connected to the cathode (ground) for N-type and to the anode for P-type of the device (MOS must be turn off). The P-substrate terminal is connected to ground. The device (anode = p-type, cathode = n-type) is proposed for snapback in the forward region. For snapback in the reverse region the NPNP must be used (anode is n-type and cathode is p-type).

Some new devices, which are realized in technology IBM BiCMOS and TSMC CMOS are similar to conventional p/n/p/n or n/p/n/p SCR, but novel devices present new cross configurations and layers dimensions enable adjustability of voltage breakdown in reverse direction, triggering voltage in forward direction, holding voltage and fulfilment of mentioned requirements. The current condition of the device is placed on instead of bulk, thereby local electrical field and a stress on the surface is eliminated. This improves the robustness of device during ESD event. The cross configuration reduces leakage current during off state. Parasitic capacitance of new device is generally less than in structures made of MOSFETs or diodes.

For this connection scheme under reverse bias condition, it can be seen that there are several forward-biased p/n junction diodes in parallel between the cathode (ground) and anode. As a result, the reverse breakdown voltage is about equal to 0,7V and the conducting current is relative high.

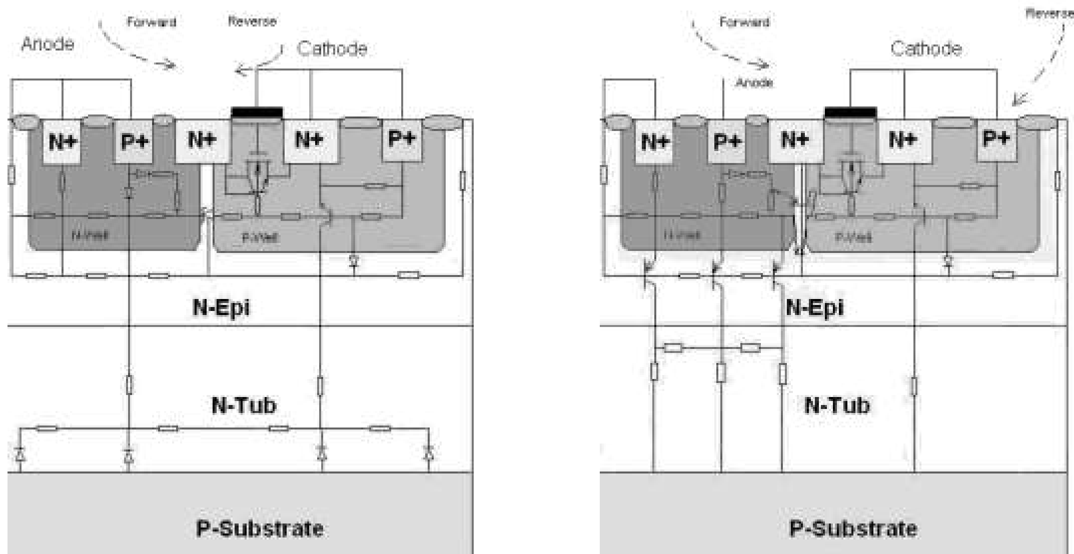

Fig 5: N-type of ESD device with N-Tub connected to anode on the left, N-type ESD device with floating N-tub on the right,[1]

For scheme from fig.5(right) under reverse bias condition, the N-tub terminal is floating, and the cathode and anode are connected internally through several shunt open-base parasitic PNP BJTs. Thus, the reverse breakdown voltage is about equal to the emitter-collector breakdown voltage of the BJTs and the conducting current is relatively low. The holding voltage can be adjusted and is most sensitive to D1, because D1 is the length of the base region of the embedded PNP bipolar transistor. The larger the D1, the smaller the current gain, and hence the larger the holding voltage.

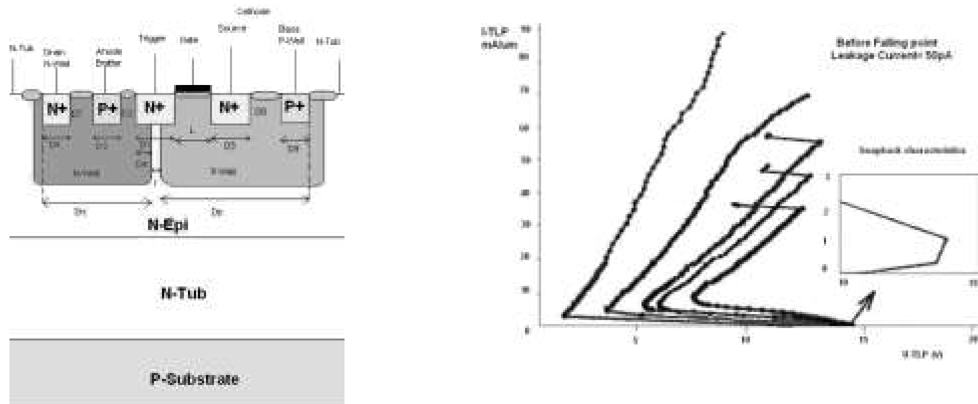

Fig 6: Above: Gate, Source (cathode) and base-P-well are connected together and trigger terminal is floating, below: Curves graph matches the table 1 values.

	L	D1	D4	D5
Curve 1	7	1,6	1,6	3,2
Curve 2	7	3,2	1,6	1,6
Curve 3	7	5,1	3,2	1,6
Curve 4	7	7,3	3,2	1,6
Curve 5	7	8	4,8	1,6

Tab 1: Values for the graph (fig.10 below). The Curve 1 is on the left, Curve 5 is on the right.

The trigger voltage and the on-state resistances can be adjusted using n- or p- type devices.

3. CONCLUSION

With the help of new advanced SCR structures is possible to tune ESD characteristics to be optimal for certain application. Such structures should be produced at the same time as core circuits to evolve with technology advancement. Optimal adjustment of silicon active areas dimensions is necessary to simulate by computer aided design systems (TCAD systems). Then can be uniquely determined which features will be given by certain dimensions setting. For applications with different requirements might be various geometrical masks of one structure produced and by this way to meet with defined requirements only using different type of mask.

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