INVERTER NON-IDELITIES AND THEIR COMPENSATION

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ABSTRACT

In the paper is described a control of inverter for low-voltage traction asynchronous drive. In case such drive is important to take into account inverter non-idealities: distortion of inverter output pole voltages by dead times and on state voltage drops on switching elements Paper deals with distortion by dead time and distortion by on-state voltage drops. Analysis and compensation methods of inverter non-idealities are described in the article.

1 INTRODUCTION

The main requirement on electric drives in independent traction is high efficiency of the driving system. Independent traction often uses low-voltage level in DC link in the drive. Typically 24 or 48 V nominal voltages of accumulators are used. Properties of low-voltage system inverter – motor are described in the paper. Knowledge of all spurious effects of this system allows us to modify control algorithms to increase the efficiency of the the driving system. The basic researched effects are non-idealities of the inverter: output voltages by dead times and distortion of inverter output voltages by on-state voltages drops at switching elements. Dead times cause harmonic distortion of inverter pole output voltage and harmonic distortion of motor voltage. The level of this distortion depends on the ratio of dead time and switching period of inverter. The impact of the first effect is independent on the voltage level on an inverter and its compensation is simpler than the second one. Compensation of this effect can be achieved in several ways. A hardware support for compensation of dead time is often implemented in DSP for inverter control. The main attention is paid to the second effect, which is more significant at low voltage levels and importantly affects inverter output voltages distortion, efficiency of the whole system and speed regularity. Harmonic distortion by on-state voltage drops is the function of duty, instantaneous current size and current polarity in each inverter pole. The smaller the inverter DC link voltage the stronger the distortion. The assumption is that the voltage drops are typically about 2.5V at inverter nominal currents. In inverters with nominal DC-link voltage is 400V and more (standard inverter). The voltage drops usually achieve 1% of this voltage. At the other hand, in inverter with low – level DC – link voltage (24V) voltage drops are about 10% and it is necessary to respect them. It can be compensated for them by correction of duty in each inverter pole. The model for compensation uses state variables (pole duty, phase currents) of the system and parameters switching components (threshold voltages and dynamic resistances of diodes and switching transistors) In addition, switching components parameters depend on temperature and the compensation is difficult to carry out exactly. The article deals with the model of inverter, which is used for compensation of presented effect in field oriented control of low voltage asynchronous drive.

2 INVERTER NON-IDEALITIES

Many inverter models use ideal switching elements (with zero switching times and zero on-state voltage drops) and constant value of DC-link voltage. In some aplication while we contol inverter is necessary to take into account real propertis of switching elements. One of this case is low voltage traction drive. In this chapter are described impacts of these effects.

2.1 IMPACT OF DC-LINK RIPPLE

When we are considering inverter as system controlled by pulse signals as inputs and pole output voltages are considered as outputs, these voltages depend on duty cycle in each pole and also on DC-link voltage.

$$U_{sk} = \left(2d_k - 1\right)\frac{U_{DC}}{2} \tag{1.}$$

DC-link obviously consist DC voltage source and capacitor with high capacitance. The course of DC-link voltage depends on hardness of the source a capacitance in DC link and on instantaneous working state of the drive. Generally this voltage isn't constant, but contains ripple. When we measure DC link voltage, it is possible to make compensation of DC-link voltage ripple effects. The simplest way of its compensation is correction of duty cycle in inverter poles.

$$d_{k,corr} = \left(d_k - \frac{1}{2}\right)\frac{U_{DC,nom}}{U_{DC,meas}} + \frac{1}{2} \tag{2.}$$

2.2 IMPACT OF DEAD TIMES AND ON STATE VOLTAGE DROPS ON INVERTER OUTPUT VOLTAGES

Finite switching times of real semiconductor elements in inverter cause necessity to delay switch on of one transistor in pole behind switching off the second one to protect DC-link against short circuit. This delay is called dead time. The configuration of one inverter pole is shown on figure 1. Switching pattern including dead time is shown on figure 2. Distortion of pole voltage depends on ratio of dead time and switching period and on sign of phase current. Distortion of pole voltage we can express as follow:

$$\Delta u_{sk} = U_{DC}\frac{T_d}{T_s}\cdot \operatorname{sgn}\left(i_{sk}\right) \tag{3.}$$

It is evident, the higher switching frequency is used, the distortion rate is higher. The dead time size is used by dynamics parameters of transistors. However, distortion by dead time is exactly given by DC-link voltage and ratio of dead time and switching period, the distortion by on-state voltage drops is function of duty cycle, phase current amplitude and sign of this current. Distortion of individual poleve voltages by on-state voltage drops we can express as follow:

$$\Delta u_{sk} = \begin{cases} u_D(i_{sk}) + d_k\left[u_T(i_{sk}) - u_D(i_{sk})\right]; i_{sk} > 0 \\ -u_T(i_{sk}) + d_k\left[u_T(i_{sk}) - u_D(i_{sk})\right]; i_{sk} < 0 \end{cases} \tag{4.}$$

Diode and transistor characteristics are possible to approximate as voltage source with internal resistance and can be expressed:

$$\begin{aligned} u_T(t) &= u_{T0} + R_T \cdot i_C(t) \\ u_D(t) &= u_{D0} + R_D \cdot i_F(t) \end{aligned} \tag{5.}$$

The distortion rate isn’t depends on DC-link voltage and the DC-link voltage is smaller, the distortion rate is higher.

In case of low voltage traction drive are these effects more affected, then common drives with DC-link voltage 400V and higher. One reason is low inductance of drive and high switching frequency is necessary for low phase currents ripples. Next, the ratio of distortion by on-state voltage drops is high in case of low voltage drive. Using modern control microprocessors is possible to make some compensation algorithms to eliminate these effects.

3 COMPENSATION METHODS OF INVERTER NON-IDEALITIES

Method for compensation of distortion by dead time must know sign of pole currents which are measured, dead time size and switching frequency which are constant or are controlled by microprocessor. This method corrects the computed duty cycles of the modulator before application to the inverter. The suitable modification of the duty cycle is:

$$d_{k,corr} = d_k + \frac{T_d}{T_s}\operatorname{sgn}(i_{sk}) \tag{6.}$$

Method for compensation of distortion by on-state voltage drops is more complicated than method for compensation of distortion by dead times. This method must by know duty cycle, amplitude and sign of pole currents and size of on-state voltage drops on each pole in inverter. The voltage drops on inverter elements are computed by equation 4. Correction of duty cycle in each pole is:

$$d_{k,corr} = d_k + \frac{\Delta u_{sk}}{U_{DC}} \tag{7.}$$

After all correction is necessary to make limitation of duty cycle values into maximal allow values for PWM modulator.

4 LABORATORY WORKPLACE

Described algorithms was implemented and validated on workplace with programmable laboratory inverter. The whole view is in figure 1. The workplace consists set of traction accumulators inverter and load which can be chosen RL-load or low-voltage induction machine and measuring instruments.

Programmable laboratory inverter contains control module with digital signal processor DSP56F803, measuring board, seven channel driving module and IGBT module

5 EXPERIMENTAL RESULT

To confirm of theoretical possibility is used laboratory workplace, with RL-load. Parameters of inverter elements used in this compensation schemes are shown in table 1.

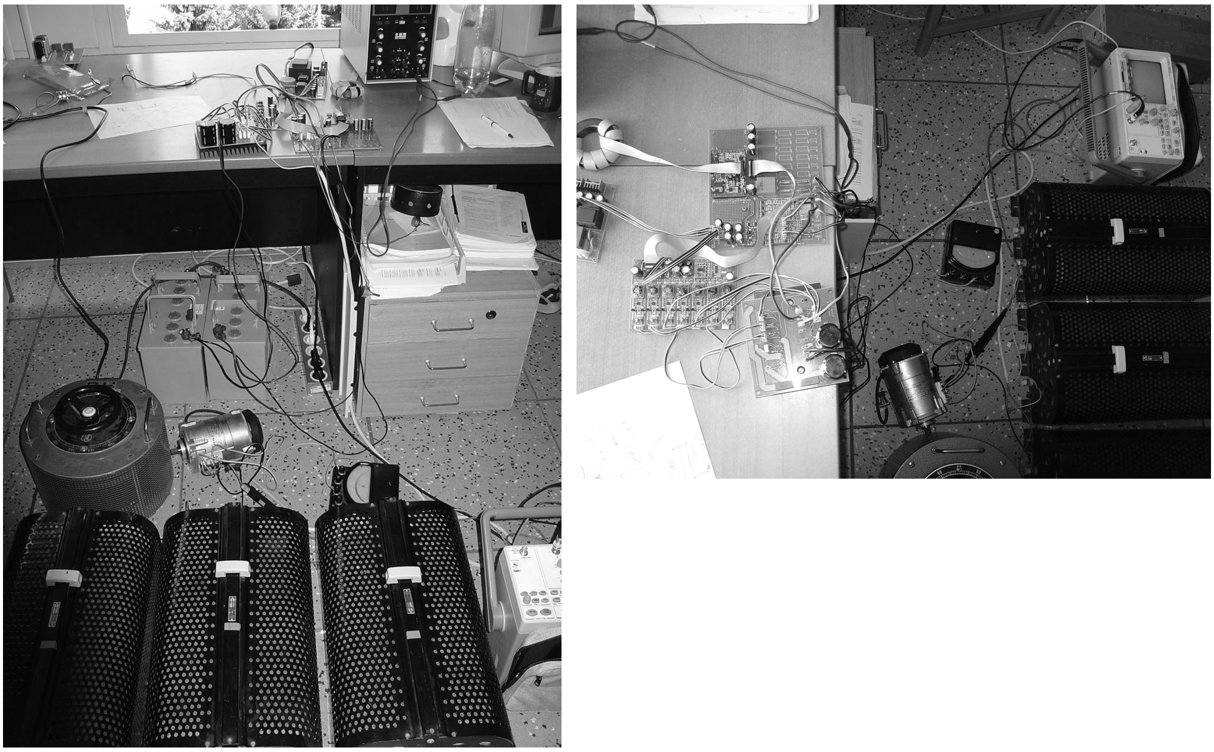

Fig. 1: *Workplace and Programmable Laboratory Inverter*

Task done during experiment was following: generation of sine wave with given magnitude and frequency to PWM module.

T_D	Effective Dead Time	$2\ 10^{-6}$ s
$U_{t,0}$	Switch On-State Voltage	1.1 V
R_t	Switch On-State Resistance	0.15 Ω
$U_{d,0}$	Diode On-State Voltage	0.82 V
R_d	Diode On-State Resistance	0.055 Ω

Tab. 1: *Inverter parameters used in compensation schemes*

There were compared impacts of particular compensation methods with uncompensated state. There were measured output currents and their higher harmonics contents. Table 2 contain signals attenuation of each harmonics, qualify in decibels. In second column are signals attenuation of harmonic on turned off compensation of voltage drops. Third, fourth, fifth columns consists signals attenuation of harmonic on turned on compensation, in this order: Dead Time compensation, Voltage Drop compensation and compensation of all distortion.

Frequency of output current is 50 Hz and switching frequency of power devices is 12 kHz.

Harmonics	Signal Attenuation			
1	-36.6	-35.7	-33.9	-33.2
2	-57.3	-61.7	-81.5	-74.8
3	-64.3	-66.3	-72.2	-68.5
5	-68.8	-68.2	-69.3	-65.0
7	-71.9	-73.6	-75.9	-78.7
9	-74.3	-73	-79.3	-81.8

Tab. 2: *Signal attenuation of harmonics*

6 CONCLUSION

Paper deals with analysis of distortions output inverter pole voltages by dead time and by on-state voltage drops on switching elements. Impact of these effects is shown. Paper also describes algorithm for compensation of these effects.

It is shown in Table 2, that amplitude of first harmonic of output current is increasing when compensation is turned on and attends to significant signal attenuation of higher harmonic. Compensation of inverter non-idealities decreases distortions of inverter output current and increases efficiency of whole system inverter – motor.

It is evident, that compensation of described effects is important especially in low voltage drives, where is necessary high inverter switching frequency which causes significant impact of dead time and low-voltage in DC-link causes significant distortion by on state voltage drops on switching elements. This is case of traction drives fed from batteries.

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