RAIL-TO-RAIL OPERATIONAL AMPLIFIER

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ABSTRACT

The lowering of the supply power and voltage has an enormous impact on the signal-to-noise ratio of analog circuit. It not only decreases because of the lower allowable signal voltages, but also because of the higher noise voltage due to the lower supply current. In order to maximize the signal-to-noise ratio, the signals have to be as large as possible, preferably from rail-to-rail. The most common method for implementing full range operation is by using a complementary differential pair. It is simply a compound structure that consists of NMOS and PMOS differential pairs connected in parallel. This paper gives an introduction to the concept of designing rail-to-rail constant gm operational amplifiers using complementary differential pair input stages.

1 INTRODUCTION

Having input and output terminals that can swing from one power supply rail to the other rail obviously makes any circuit more attractive, whether the power supply is l0V, 5V, or 2V. Naturally, one can find many publications on op-amps with such circuit characteristics both in bipolar and in CMOS technologies. In these op-amps, an n-channel differential pair and a p-channel differential pair are used in parallel as shown in Figure 1.

This technique enables the input stage to operate rail-to-rail. There are basically three operation regions:

Region I. When V_{CM} is close to the negative rail, VSS, only p-channel pair operates. The n-channel pair is off because its V_{GS} is less than V_T. The total transconductance of the differential pair is given by $g_{mT} = g_{mp}$.

Region II. When V_{CM} is in the middle range, both of the p-and n-pairs operate. The total transconductance is given by $g_{mT} = g_{mn} + g_{mp}$.

Region III. When V_{CM} is close to the positive rail, only n-channel pair operates. The total transconductance is given by $g_{mT} = g_{mn}$.

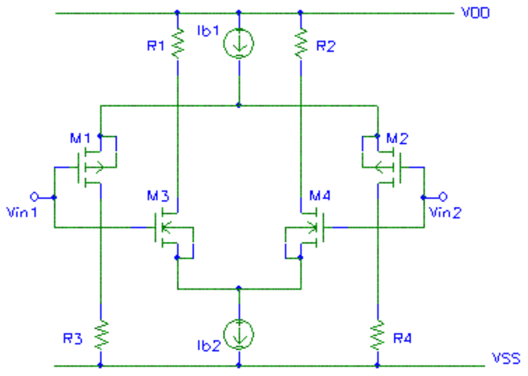

Fig. 1: *Rail-to-rail input stage in CMOS and bipolar implementations.*

It is desirable to maintain the nominal performance of the circuit for the entire common mode input range. One of the most important circuit parameters is the transconductance, g_m, of the input stage. The total input stage transconductance, g_{mT} of the circuits in Figure 1 is given by the sum of the transconductance of the n- and p-channel (or-type) differential pairs, g_{mn} and g_{mp}, respectively. Since there are three regions of operation for the input stage, there are three different regions for the g_{mT}. Figure 2 shows the transconductance of the rail-to-rail CMOS input stage as a function of V_{CM}. MOS transistors operating as current sink/source are used to respectively provide In and Ip for the simulation since an ideal current source will not turn off regardless of the voltage drop across it. Drain terminals of the n- and p-channel differential pairs are connected to V_{DD} and V_{SS}, respectively, for the simulation since we are only interested in g_m of the differential pairs. Since the output drain currents of the n- and p-pairs will eventually be added up, the total transconductance is given by: $g_{mT} = g_{mp} + g_{mn}$

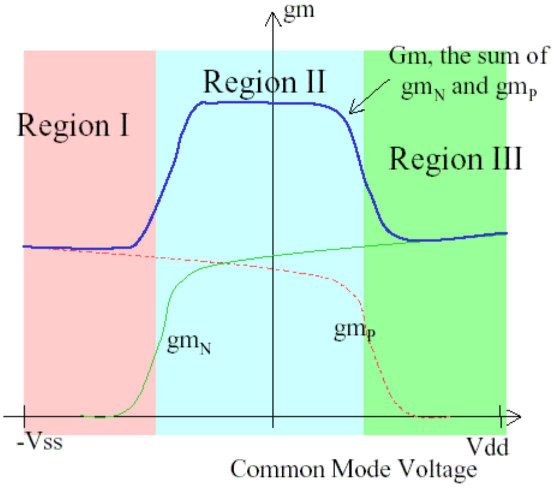

Fig. 2: *Transconductance of a rail-to-rail CMOS input stage as a function of CMR.*

If the nominal values of g_{mn} and g_{mp} can be matched, then the ratio of the maximum value of g_{mT} (when both pairs are working) to the minimum value (only one pair is working) is two. The change in g_{mT} with V_{CM} as depicted in Figure 2 is not desirable, the main reason is:

Constant bandwidth: for single-stage amplifier and two-stage Miller compensated amplifier, the unity gain frequency (UGF) is proportional to g_{mT} of the input stage. Non-constant UGF affects both the speed of circuits and also noise bandwidth.

In order to overcome the afore-mentioned drawback of rail-to-rail input stages, their transconductance has to be regulated at a constant value. The next section describes the design of these types of input stages.

2 CONSTANT-G$_M$ RAIL-TO-RAIL INPUT STAGES

The rail-to-rail folded cascode input stage, as shown in Figure 1, can be biased either in weak or in strong inversion. If it operates in weak inversion, the total transconductance is given by

$$g_{mT,weak} = g_{mp,weak} + g_{mn,weak} = \frac{I_p}{2n_p V_{th}} + \frac{I_n}{2n_n V_{th}} \tag{1}$$

Where I_p is the tail current of the p-channel input pair and I_n is the tail current of the n-channel input pair, and the V_{th} is the thermal voltage kT/q which is about 26 mV at room temperature, and n is the weak inversion slope factor.

As can be concluded from this formula, the g_{mT} of MOS transistors operating in weak inversion only depends on the tail current I_p and I_n. If a transistor requires a large transconductance, for example to achieve a certain high-frequency performance, the tail current of the transistor has to be increase. However, if the tail current is increased too much, the transistor ends up in strong inversion.

If the input stage is biased in strong inversion, then the total g_{mT} is given by:

$$g_{mT,strong} = g_{mp,strong} + g_{mn,strong} = \sqrt{2(K_p \frac{W}{L}) I_p} + \sqrt{2(K_n \frac{W}{L}) I_n} \tag{2}$$

Where K_p and K_n are the transconductance parameters of the p- and n-channel input transistors. And it is given by

$$K_{p,n} = \mu_{p,n} C_{ox} \tag{3}$$

From expression 1 it can be concluded that the g_{mT} of a rail-to-rail input stage operating in weak inversion can be controlled by changing the tail currents of the input transistors. In strong inversion, the g_{mT} can be regulated by either changing the tail currents, the gate-source voltages or even the W over L ratios of the input transistors, as can be concluded from the expressions 2 and 3.

Basically there are three different methods to control the transconductance of a rail-to-rail input stage. They control: the tail currents of the input pairs; the gate-source voltages of the input transistors; and the W over L ratio of the input transistors. In the next sections rail-to-rail input stages will be described which have a constant g_{mT} over the entire common-mode input range. These constant g_{mT} rail-to-rail input stages can operate in either weak or strong inversion.

2.1 RAIL-TO-RAIL INPUT STAGES WITH CURRENT-BASED G_M CONTROL

In this section, some methods are discussed which make the g_{mT} of a rail-to-rail input stage constant by regulating the tail currents of the complementary input pairs. Subsequently, constant g_{mT} input stages operating in weak and strong inversion will be addressed.

2.1.1 ONE-TIMES CURRENT MIRROR TECHNIQUE

In weak inversion the g_m of an MOS transistor is proportional to its drain current. This indicates that the g_{mT} of a rail-to-rail input stage operating in weak inversion can be made constant by keeping the sum of the tail currents of the complementary input pairs constant. Thus for a constant g_{mT}, the sum of tail currents has to obey the following expression

$$I_p + I_n = I_{ref} \tag{4}$$

Where it is assumed that the weak inversion slope factors of both transistor types are equal. The above-mentioned principle is realized in the rail-to-rail input stage as shown in Figure 3. It consists of complementary input pairs M_1-M_4, and a summing circuit M_5-M_{10}. The g_{mT} control of the input stage is implemented by means of the current switch M_{13}, and the current mirror M_{11}-M_{12}. If low common-mode input voltages are applied to this input stage, the current source, I_{ref}, biases the p-channel input pair. As a consequence, the p-channel input pair can process the input signal. If the common-mode voltage is now raised to about V_{DD}-V_{b3}, the current switch M_{13} takes away a part of the current I_{ref} and feeds it through the current mirror M_{11}-M_{12}, into the n-channel input stage. In this way, the sum of the tail currents of the input pairs is kept equal to I_{ref} which immediately follows from applying Kirchhoff's current law to the common-source node of the p-channel input pair.

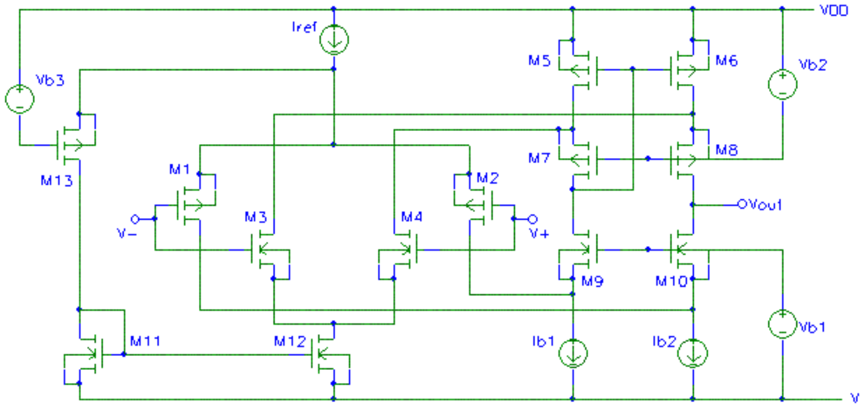

Fig. 3: *Rail-to-rail input stage with one-times current mirror technique.*

2.1.2 THREE-TIMES CURRENT MIRROR TECHNIQUE

The transconductance of a rail-to-rail input stage operating in strong inversion can be made constant by keeping the sum of the square roots of the tail currents of the complementary input pairs constant, as readily follows from equation 2. This yields

$$\sqrt{I_p} + \sqrt{I_n} = 2\sqrt{I_{ref}} \tag{5}$$

A brute-force implementation of equation 5 is applied to the rail-to-rail input stage as shown in Figure 4. The input stage consists of a rail-to-rail input stage, M_1-M_4, and a folded cascode summing circuit, M_5-M_{10}. The g_m of this input stage is regulated by means of two current switches, M_{13} and M_{16}, and two current mirrors, M_{11}-M_{12} and M_{14}-M_{15}, each with a gain of three. For the sake of simplicity, this current mirrors will be called three-times current mirrors, in the remaining part of this section. In the intermediate part of the common-mode input range both current switches are off. The result is that the complementary input pairs are biased with a current of $I_{ref.}$ And thus the tail currents obey expression 5, in this part of the common-mode input range.

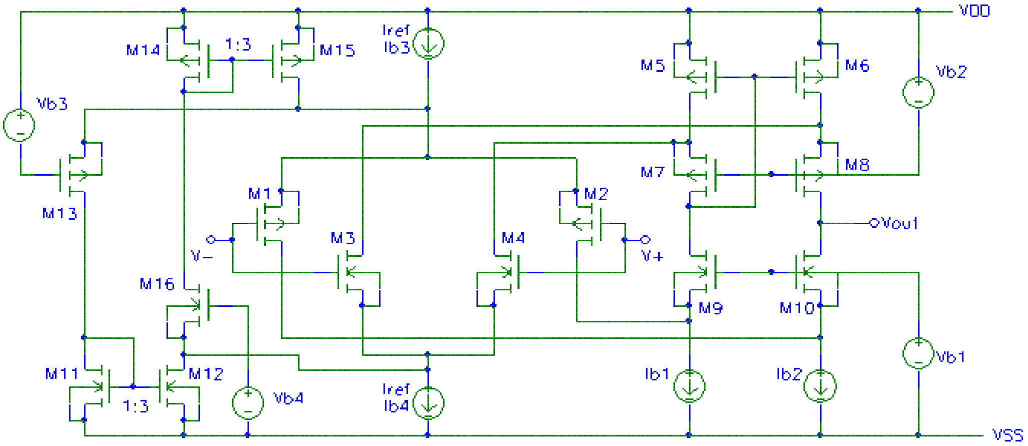

Fig. 4: *Rail-to-rail input stage with gm control by two three-times current mirrors.*

If the common-mode input voltage decreases below V_{b4}, the current switch, M_{16}, takes away the tail current of the n-channel input pair and feeds it into the current mirror M_{14}-M_{15}. Here it is multiplied by a factor three and added to the tail current of the p-channel input pair. The result is that the tail current of the p-channel input pair is equal to 4 $I_{ref.}$ Since the tail current of the n-channel input pair is zero in this part of the common-mode input range, equation (5) is fulfilled. Similarly, it can be explained that, for large common-mode input voltages, the g_m control regulates the tail current of the N-channel input pair at a value of 4 I_{ref}. As a consequence, the tail currents again comply with expression 5.

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REFERENCES

[1] Satoshi, S. J, et al.: Low-Voltage CMOS Operational Amplifiers, 1995, ISBN: 0-7923-9507-7.

[2] Hogervorst, R. et al.: Design Of Low-Voltage, Low-Power Operational Amplifier Cells, 1996, ISBN: 0-7923-9781-9.

[3] Francisco Duque-Carrillo. 1-V Rail-to-Rail Operational Amplifiers in Standard CMOS Technology, IEEE Journal of Solid-State Circuits, vol. 35, pp. 33 - 44, January 2000.