PLL FREQUENCY SYNTHESIZER FOR L-BAND SATELLITE RECEIVER

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ABSTRACT

The frequency synthesizer of an L-Band Front End for the new AMSAT Phase 3E satellite is described. High reliability and low power consumption of the receiver is required. For slow rate data transmissions high stable oscillators in the double conversion receiver are required and retuning of the first oscillator is needed. The invention of the receiver design consists in utilization of the double PLL synthesizer synchronized by an ultra stable oscillator positioned onboard the satellite.

1 INTRODUCTION

The synthesizer is developed as a part of an L-band front-end on-board a satellite. Requirements for the front-end are very high. Besides high reliability in the temperature range –30 up to +40 degrees, mechanical resistance and low power consumption, the requirement for high frequency stability is important. The reason for that is given by exigency of low data rate transmission in both the coherent and non-coherent modes [1]. Next requirement results from ESA Galileo project. The experimental traditional satellites frequency of 1268 MHz is allocated as downlink frequency for Galileo space segment as well. We have to make calculations with a possible receiver retuning of 1260 MHz. These are the reasons why we have decided to develop the L-band front end, based on the double PLL frequency synthesis procedure.

2 CONCEPTION OF SATELLITE ON-BOARD L-BAND RECEIVER SYNTHESIZER

The standard design of local oscillators in microwave receivers utilizes a chain of frequency multipliers with a high stability quartz oscillator at a low frequency of tens to a hundred MHz. This concept promises good spectral purity close to a carrier. But this solution has significant disadvantages like high power consumption, large dimensions and low efficiency. Frequency switch over may also be very difficult.

In our application we need two oscillators for the dual conversion L-band receiver. The first oscillator frequency is 1096.61 MHz with a possibility to switch over to 1088.11 MHz according to a command from the ground. The second oscillator is fixed at 182.77 MHz. The receiver should be able to process very slow data rate (from 20 up to 400 bps) PSK signals. The spectral purity close to a carrier needs to be high. Another way is to utilize a frequency synthesizer. The following advantages over a chain of multipliers may be expected: possibility

of tuning, only one reference frequency for all coherent output frequencies, lower current consumption (less than 5 mA) and smaller dimensions. The main disadvantage is worse spectral purity near a carrier. High reliability of the receiver is very important. The simplest solution is to use a parallel controlled synthesizer with a memory containing data for synthesizer registers. The MC145152 manufactured by Motorola® is one of few such devices currently available. The block diagram of MC145152 is shown in fig. 2.

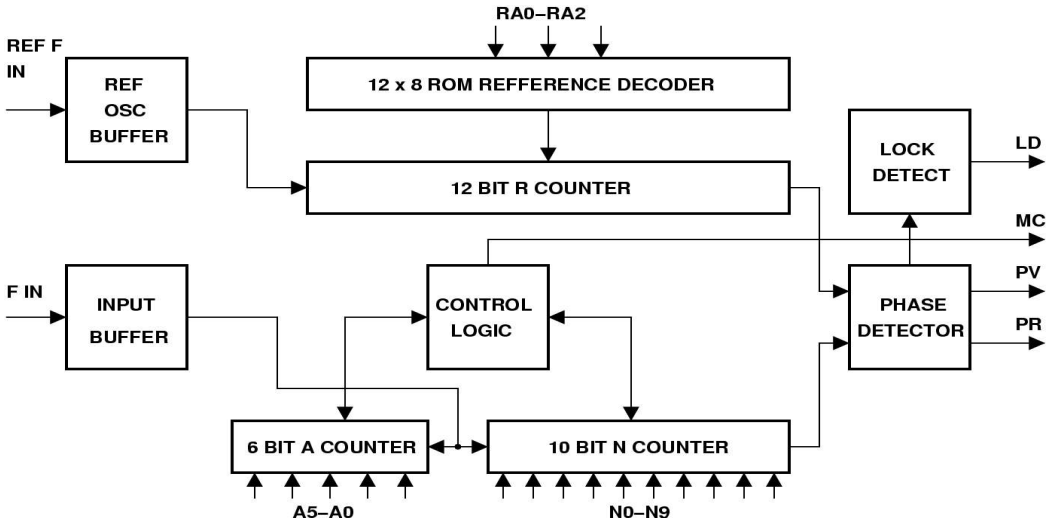

Fig. 2: *Functional block diagram of the parallel synthesizer MC145152*

In the SO-28 package, a phase detector, counters, reference oscillator with buffer, and lock detection circuit are included. A fast ECL prescaler and a charge pump must be external. This synthesizer needn't a controller because frequency is set-up permanently. The retuning of the 1 GHz oscillator is done with help of simple static combination logic. This solution has high interference immunity but demand two synthesizers with external charge pumps and prescalers. So it leads to increasing dimensions and current consumption.

2.1 SERIAL CONTROLLED DUAL SYNTHESIZER

The second solution uses modern monolithic dual integrated synthesizer LMX1601 from National Semiconductor®. This part has been designed to be used in a local oscillator subsystem for a radio transceiver. The LMX1601 includes two dual modulus prescalers (1.1 GHz and 500 MHz), four programmable counters and two selectable gain charge pumps. Digital filtered lock detects for both PLLs are included. Data are transferred into the synthesizer by a three wire serial interface. Internal structure is shown in fig. 3.

Low current consumption at low supply voltage and small dimensions (TSSOP-16 package) are the main advantages of this part. Both PLLs are independently programmable. It means that dividing ratios of all prescalers and charge pump gains are separated. Only a reference frequency input is common for both PLLs. The frequency of the ultra stable oscillator (USO) placed on the satellite board is 5 MHz. The LMX1601 contains single programmable (by Microwire™ serial interface) 18-bit data register for all of the four internal counters. The lock detector indicates the lock state of both the PLLs. The controller is PIC12C508 from Microchip® chosen for its small package (SO-8) and low current consumption. The synthesizer and the controller have the same supply voltage of 3 V. The Main PLL section operates up to 1100 MHz and it is used for the first tunable local oscillator at 1096.61 or 1088.11 MHz. The

Aux PLL section operates up to 500 MHz and is used for the second fixed local oscillator at 182.76 MHz. The internal references for both the PLLs have been selected as a compromise between minimal differences of the required output frequencies and spectral purity of the generated signal. The requirement of synthesizer high reliability has already been mentioned above.

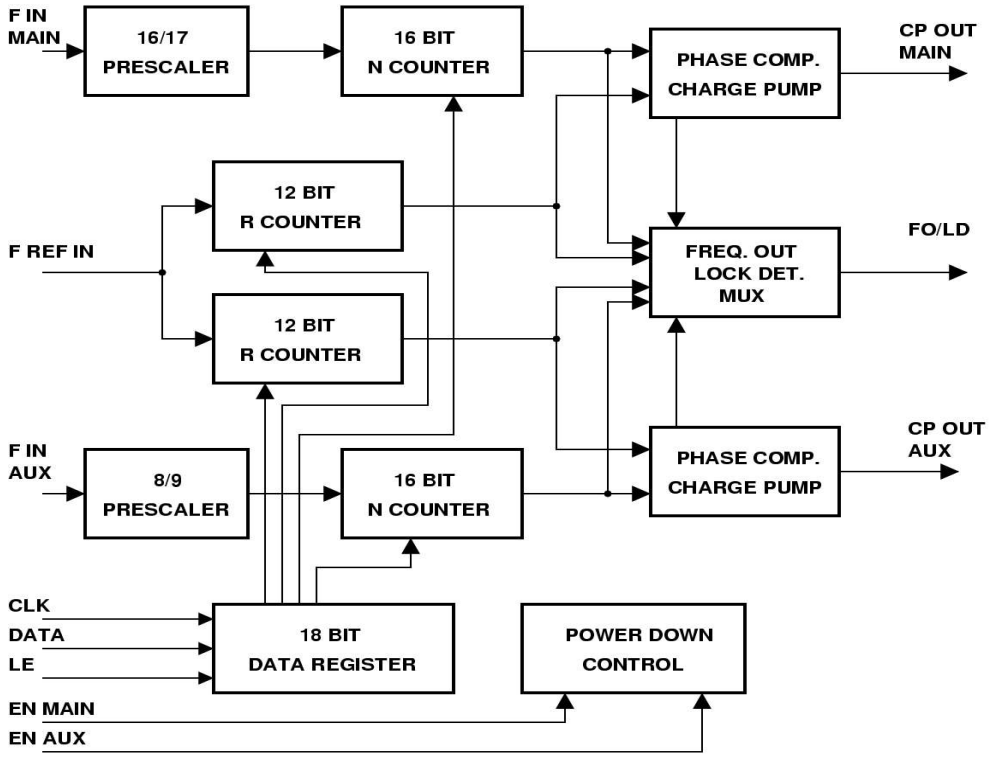

Fig. 3: *Functional block diagram of the dual synthesizer LMX1601*

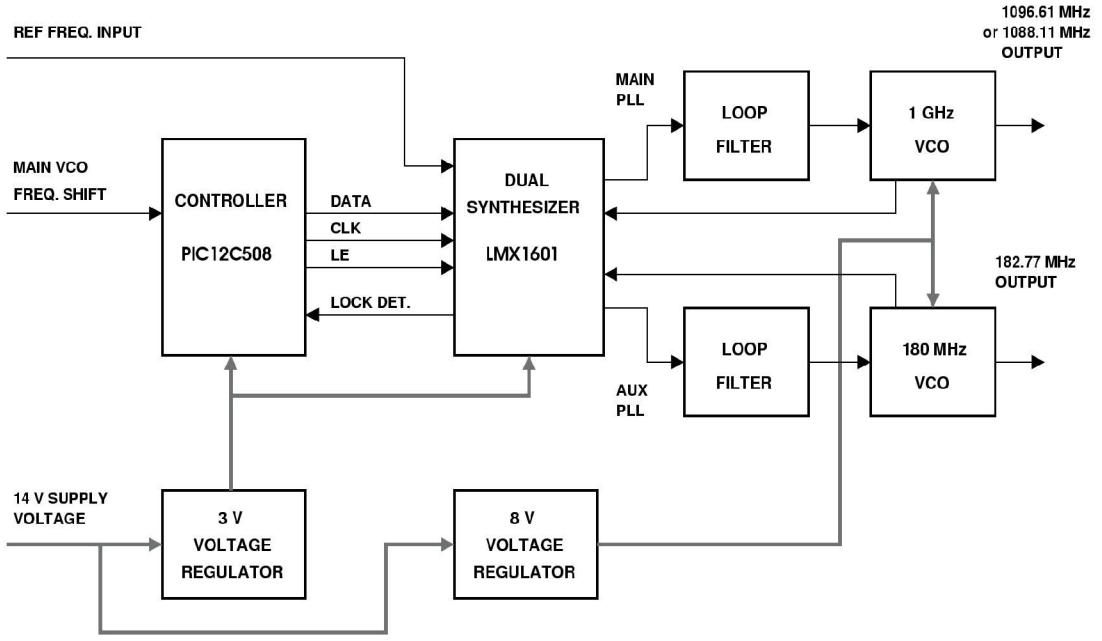

Fig. 4: *Application block diagram of the dual synthesizer*

A code for the controller has to provide a repeated data loading to the synthesizer, independent of other satellite operations. In the program loop, controller's frequency shift input is tested. If the logic level is low, the frequency of the Main VCO is changed from 1096.61 MHz to 1088.11 MHz. The program of the controller has to be simple and resistant to random interferences that could occur on board the satellite. The configuration data are loaded when the L-band receiver will be switched on. Of course, the data loading needs to be repeated every time one of the loops gets unlocked too. But we also have to assume a soft damage to the registry contents (e.g. by radiation). For this reason the data could be loaded at a regular interval. At present, we consider about synthesizer's optimal control sequence. Principle of the controlled synthesizer is shown in fig. 4.

The PLLs need to be designed for low phase noise near a carrier because it is a part of the slow rate data PSK receiver. Lock time can be long because the synthesizer will not be tuned during operation. To minimize the low frequency phase noise, bandwidth of the loop filter should be very narrow. From the phase noise point of view, the connection between loop filter and varactor could also be a critical point [2]. A typical configuration for 1 GHz oscillator is shown in fig. 5.

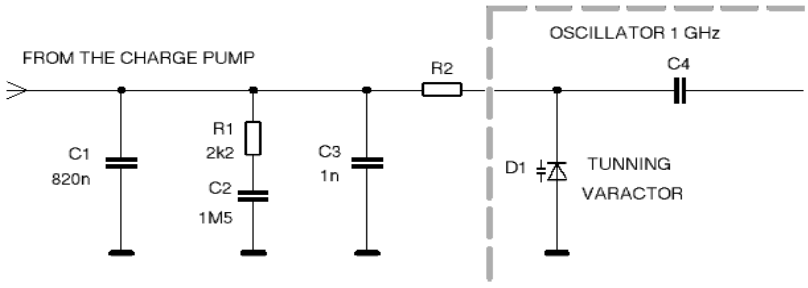

Fig. 5: *A loop filter and connection to an oscillator varactor*

2.2 SIMULATION

We have designed a second-order type loop filter. The third time-constant represented by R2 and C3, is very short compared to time constants T1 and T2.

$$T1 = R1 \cdot C2 \quad (1) \qquad T2 = R1 \cdot C1 \cdot C2 / (C1 + C2) \quad (2)$$

The value of R2 should be small for good noise parameters. Synthesizer's PLL loop have been simulated in National Semiconductor® WEBENCH™ tool Easy PLL [3]. Other parameters such as VCO, XO constants (gain, noise floor), filter components and tolerances have been defined. We have selected a comparison frequency of 50 kHz as large as possible because of VCO output-frequency accuracy. The charge pump gain is about 1 mA, VCO gain on 1 GHz side is 10 MHz/V and 2 MHz/V on 182 MHz side. Loop bandwidth of both PLLs is 100 Hz.

Loop filter time constants	T1 = 3.3 ms, T2 = 1.7 ms	see fig. 5
Phase noise, 50 Hz offset	–69 dBc/Hz	VCO noise = –140 dBc/Hz TCXO noise = –180 dBc/Hz 10 kHz offset
Phase noise, 1 kHz offset	–107 dBc/Hz	
Phase noise, 10 kHz offset	–139 dBc/Hz	
Lock time	62 ms	

Tab. 1: *Results of the 1 GHz PLL side simulation*

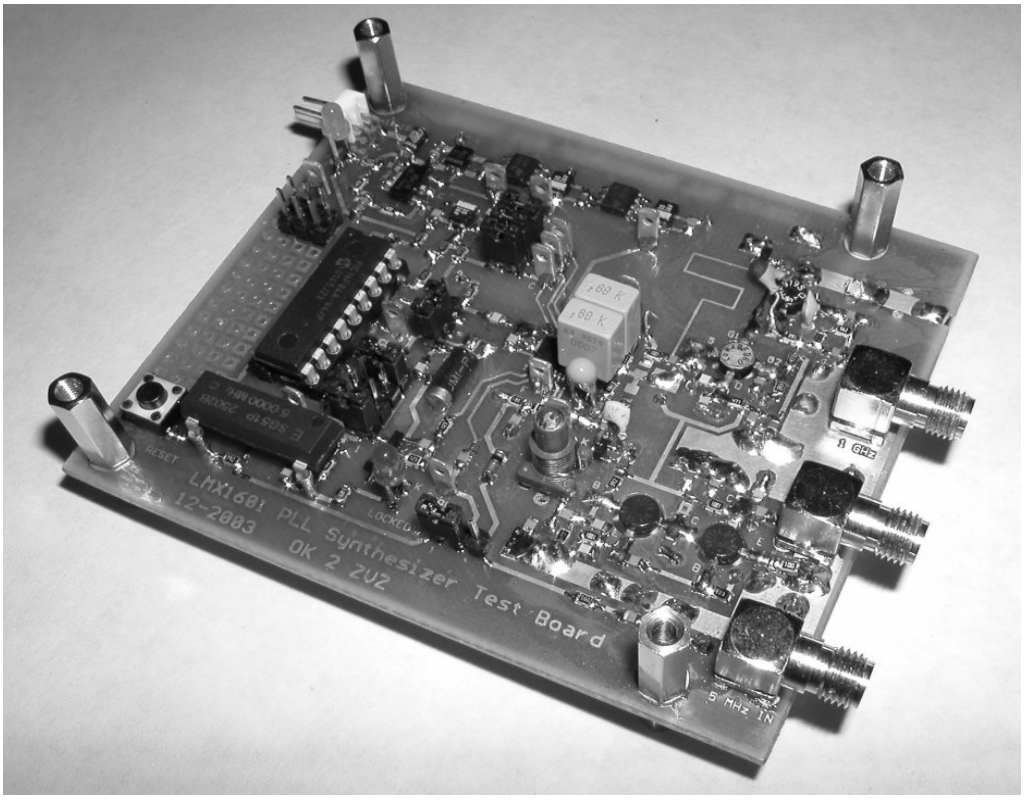

Fig. 6: *The LMX1601 PLL synthesizers test board*

3 CONCLUSION

Experiments include measurements of phase noise and reliability of the controller program and all circuits of the synthesizer. There is a supposition that the 1 GHz synthesized signal should be more critical in comparison to the 182 MHz signal. However, the phase noise accompanying both signals will be uncorrelated and added at the receiver signal outputs. These experiments are at an initial stage.

ACKNOWLEDGEMENTS

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