# MEASUREMENT OF CAPACITANCES BASED ON A FLIP-FLOP SENSOR

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## ABSTRACT

This paper deals with a new type of system for measuring capacitances with the use of a flip-flop sensor controlled by a so-called fast-rise current control pulse. The theoretical considerations are compared with experimental results, and good agreement is reported.

#### **1** INTRODUCTION

The circuit in Fig.1 was introduced in [1] as a flip-flop sensor. The flip-flop sensor is part of a class of silicon sensors with a digital output. A standard flip-flop consisting from two transistors and two resistors (see Fig.1) is characterized by two stable states, 1 and 0.

One of the authors of the patent flip-flop sensor was Lian [1], who showed that a flipflop sensor can be used for measuring non-electrical quantities and derived a formula for calculating the equivalent voltage of the flip-flop sensor controlled by a slow-rise control pulse. The principle of measurement is based on the measured non-electrical quantity breaking the value symmetry of the inverters relative to the morphological symmetry axis passing through points K and Z (see Fig.1).

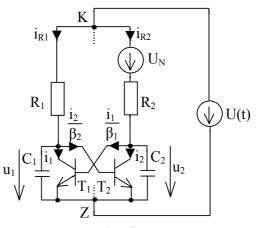


Fig. 1:Flip-flop sensor

However measured quantity can be compensated by a voltage  $U_N = U_{NE}$  in such a way that by repeated connection to source I(t) the 50% state [1] is restored, so that the magnitude of the measured non-electrical quantity will be reflected in the voltage  $U_{NE}$ , which we will call the equivalent voltage. However, it is not necessary to stick to the custom of using sensorial elements, as shown in Fig.1.

It should be noted that in current control we also distinguish between pulses with a fast or slow-rise segment of the control pulse (see Fig.2).

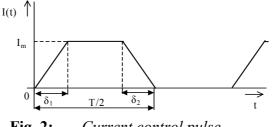


Fig. 2: Current control pulse

Control with a fast-rise segment of the control pulse is characterized by the ratio  $I_m/\delta_1$  being such that the currents passing through the capacitors are not negligible compared to the transistor currents of the flip-flop sensors. This notion should be understood in its relative sense. In practice, this condition is satisfied if  $\delta_1, \delta_2 << R_1C_1$  and  $\delta_1, \delta_2 << R_2C_2$  at the same time.

The goal of this paper is to show that capacitors can be measured with the use of a flipflop sensor in the structure of an auto-compensative system [2,3].

## 2 EQUIVALENT VOLTAGE

As described above, the asymmetry of the flip-flop sensor can be compensated by the equivalent voltage  $U_{NE}$  [1]. If we assume mismatches in the capacitances  $C_{I}, C_{2}$ , then the formula for the equivalent voltage has the form [2,3]:

$$U_{NE} = \frac{R\Delta C}{2C} I_m \tag{1}$$

where  $I_m$  is an amplitude of the current control pulse,  $C_1 = C + \Delta C$ ,  $R = R_1 = R_2$ ,  $C_2 = C$  and  $\Delta C / C \ll 1$ .

The formula for calculation of equivalent voltage of flip-flop sensor controlled by vertical rise segments of the control pulse was first derived by Kollár [2,3].

#### **3** AUTO-COMPENSATIVE SYSTEM

An auto-compensative system is shown in Fig.3.  $R_1$  and  $R_2$  are the load resistors of the flip-flop and usually range from a few k $\Omega$  to tens of k $\Omega$ s.  $R_k$  is small resistor its value is normally two orders of magnitude smaller than  $R_1$  and  $R_2$ . The voltage  $u_0$  is attenuated by the ratio  $R_0/R_k$  ( $R_0 >> R_k$ ) and is fed to flip-flop sensor. By adjusting  $u_0$ , the asymmetry due to components in the flip-flop can be compensated, thus bringing the flip-flop sensor into 50% state [1]. The two outputs of the flip-flop are connected to comparators and the comparator outputs are connected to the integrator and reversible counter. The current of the flip-flop is switched on and off by a pulse generator. It is obvious that feedback is realized as analog, but

reversible counter connected to the comparators enables to represent measured capacitance in digital form.

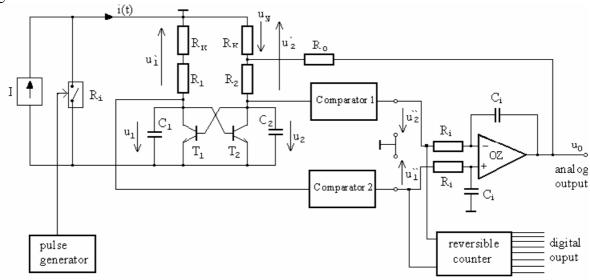


Fig. 3: Auto-compensative system

The principle of the auto-compensative system functioning is in more detail described in references [2,3].

## **4 PROPOSED SOLUTION**

Experimental circuit was made by surface montage technology. Fig.4 shows an experimental circuit. The parameters were set as follows  $R=6.8k\Omega$ ,  $R_k=10\Omega$ ,  $R_0=1.8$  k $\Omega$ ,  $C_i=10$  nF,  $R_i=10$  k $\Omega$  and C=530 pF. The flip-flop sensor was controlled by a current pulse according to Fig.2, while  $\delta_1 = \delta_2 = 100$ ns,  $I_m = 0.83$  mA and T=100µs.

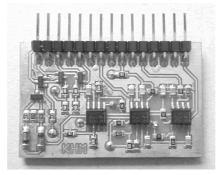


Fig. 4: A photography of experimental circuit

An important parameter of the flip-flop sensor is offset voltage. Let the offset voltage depends on temperature changes, mismatches in resistances and capacitances, mismatches in transistor saturation currents and current gains. Assume that the two transistors are subjected to the same temperature and that the effect of mismatches in the transistor saturation currents and current gains and of mismatches in the resistances of the flip-flop is negligible compared with the effect of mismatches in the capacitances of the flip-flop sensor. The major cause of offset voltage is then due to mismatches in the capacitances of the flip-flop sensor. An

asymmetry caused by mismatches in capacitances we will call a capacitive offset. A capacitive offset  $\Delta C_1$  can be compensated by a small DC voltage, or by a small capacitance to achieve  $C_1=C_2$ .

Now suppose that measured capacitance  $\Delta C_2$  is parallel connected to capacitance  $C_1$ . The capacitance  $\Delta C_2$  can be calculated using formula [2,3]

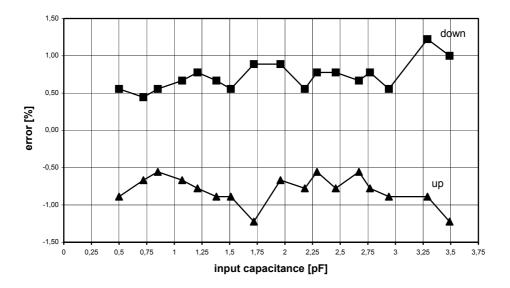
$$\Delta C_2 = \frac{2U_{NE}C}{RI_m} - \Delta C_1 \tag{2}$$

where  $U_{NE}$  is equivalent voltage with offset. The formula (2) was derived through (1) under the condition that  $\Delta C = \Delta C_1 + \Delta C_2$ , where  $\Delta C_1$  represents a capacitive offset.

The idea to measure the capacitances with compensation of the offset was used in the experiment. First must be measured capacitive offset  $\Delta C_1$  and then measured capacitance  $\Delta C_2$  can be calculated using (2). As shown above, the principle of operation is based on the measured capacitance breaking the value symmetry of the flip-flop, but the equivalent voltage can compensate this. In this case, the asymmetry will be reflected in the number of pulses read by the reversible counter. The capacitance will be equivalent to the mean number of the pulses read. In the practical measuring, the number of pulses read was processed using microprocessor and measured capacitance was calculated using formula (2) in Lab VIEW.

#### **5 METROLOGICAL CHARACTERISTICS**

To use the system in an industry applications its metrological characteristics must be known. In accordance with norm IEC 770, Fig.5 shows achieved errors for the change input capacitance from 0.5 pF to 3.5 pF (up) and from 3.5 to 0.5 pF (down). Input capacitances were made from phone cable given distances [4], and measured by RLCG meter BM 590.



**Fig. 5:** Achieved errors for the change input capacitance up and down in percents from measuring range (3 pF).

From Fig.5 it follows that maximal value of hysteresis is equal to 2,22 % for input capacitance 3,5 pF. The value of repeatability is equal to 0,0205% for input capacitance 2.75 pF.

# 6 CONCLUSION

In this paper, a new method, based on a flip-flop sensor, for measurement capacitances in range a few pF has been presented. Auto-compensative system with flip-flop sensor enables to set the equivalent voltage automatically. To measure a capacitance connected to flip-flop, pulses from inverters are processed in reversible counter. A number of the pulses read represents a measured capacitance  $\Delta C_2$ . But the flip-flop has a capacitive offset. To avoid incorrect measurement, capacitive offset  $\Delta C_1$  must be measured. Then capacitance  $\Delta C_2$  to be measured can be calculated using formula (2) in Lab VIEW. Fig.7 shows photography of measuring system. Measuring range can be changed with the values of load resistors R, current amplitude  $I_m$  or capacitance C, respectively, but it has not been investigated in this paper.

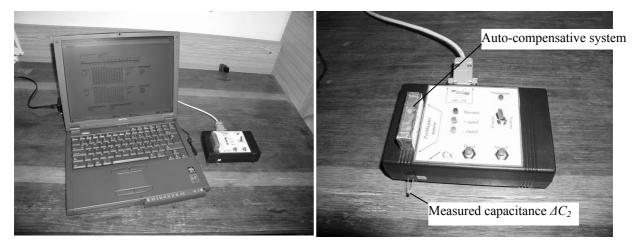


Fig. 6: A photography of measuring system

# ACKNOWLEDGEMENTS

The work presented in this paper was supported by Grant of Ministry of Education and Academy of Science of Slovak republic VEGA under Grant No.1/9030/02.

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